FIG. 1

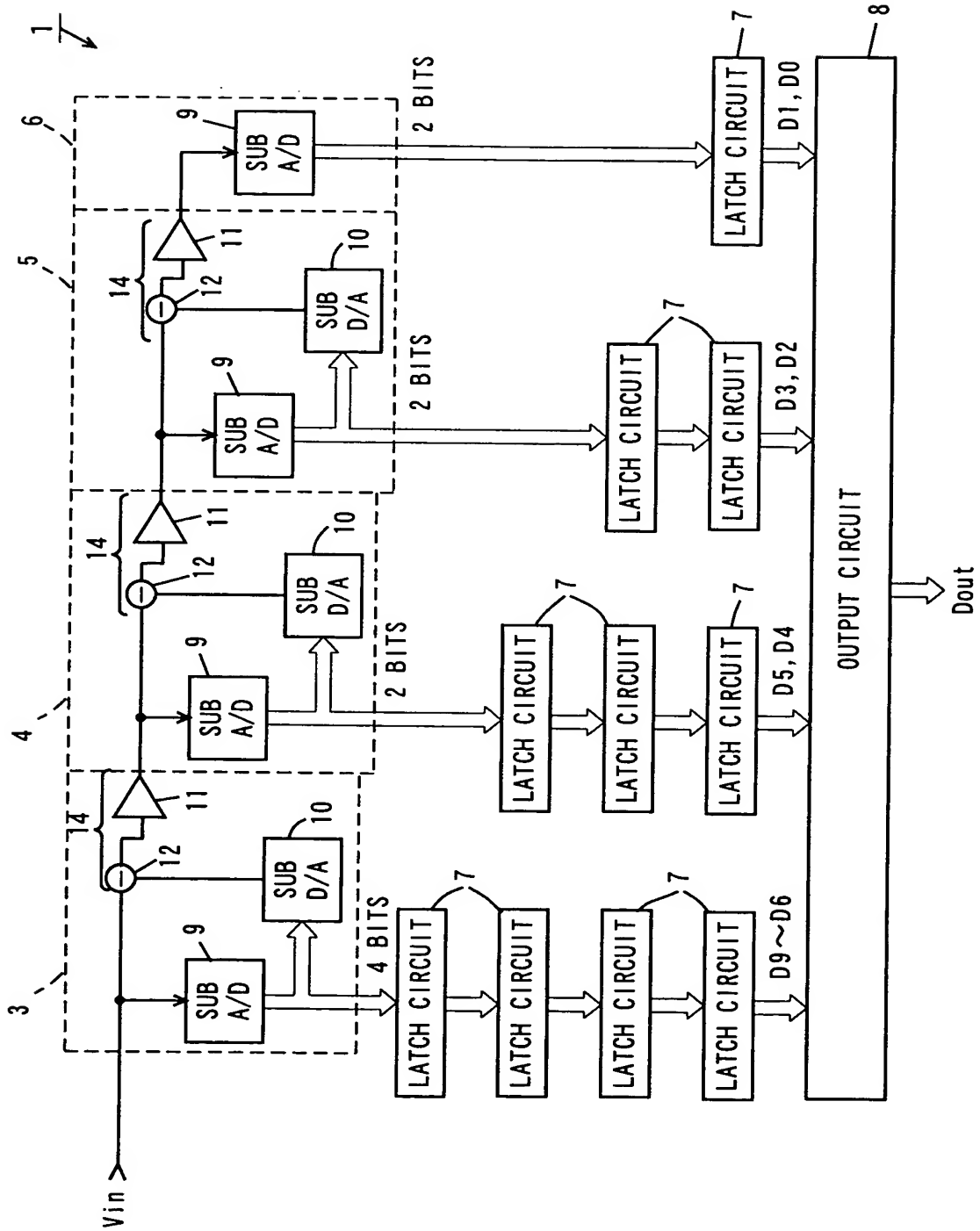

1
6
5
4
3
9
SUB A/D
10
SUB D/A
11
12
14
2 BITS
4 BITS
7
LATCH CIRCUIT
D1, D0
D3, D2
D5, D4
D9~D6
8
OUTPUT CIRCUIT
Dout
Vin

FIG. 2

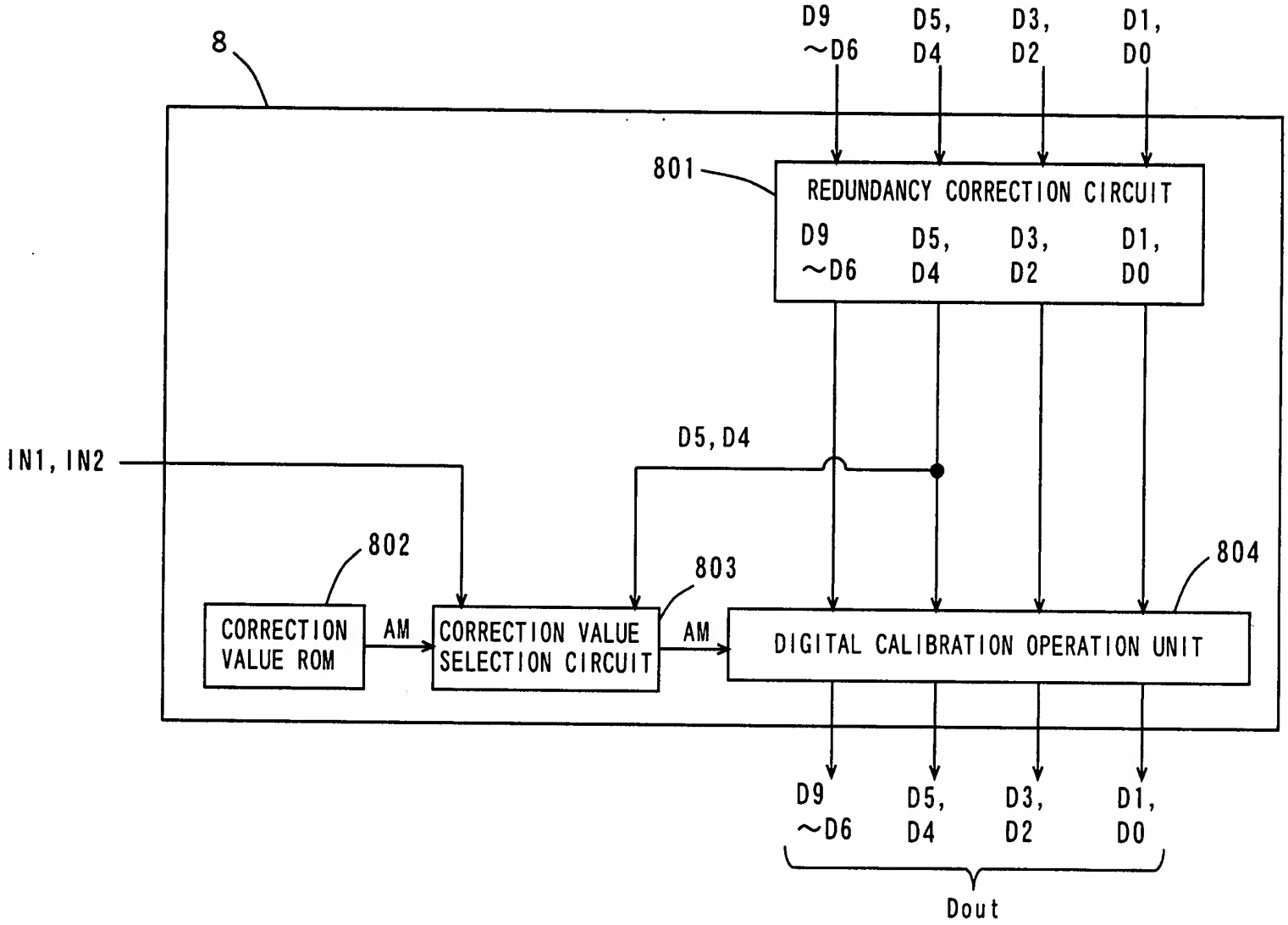

8
D9 ~D6
D5, D4
D3, D2
D1, D0
801
REDUNDANCY CORRECTION CIRCUIT
D9 ~D6
D5, D4
D3, D2
D1, D0
IN1, IN2
D5, D4
802
803
804
CORRECTION VALUE ROM
AM
CORRECTION VALUE SELECTION CIRCUIT
AM
DIGITAL CALIBRATION OPERATION UNIT
D9 ~D6
D5, D4
D3, D2
D1, D0
Dout

FIG. 3

TBL

		DC CONTROL SIGNAL IN1, IN2			
D5	D4	0, 0	0, 1	1, 0	1, 1
1	1	00 (0)	01 (1)	10 (2)	11 (3)
1	0	00 (0)	01 (1)	01 (1)	10 (2)
0	1	00 (0)	00 (0)	01 (1)	01 (1)
0	0	00 (0)	00 (0)	00 (0)	00 (0)

FIG. 4

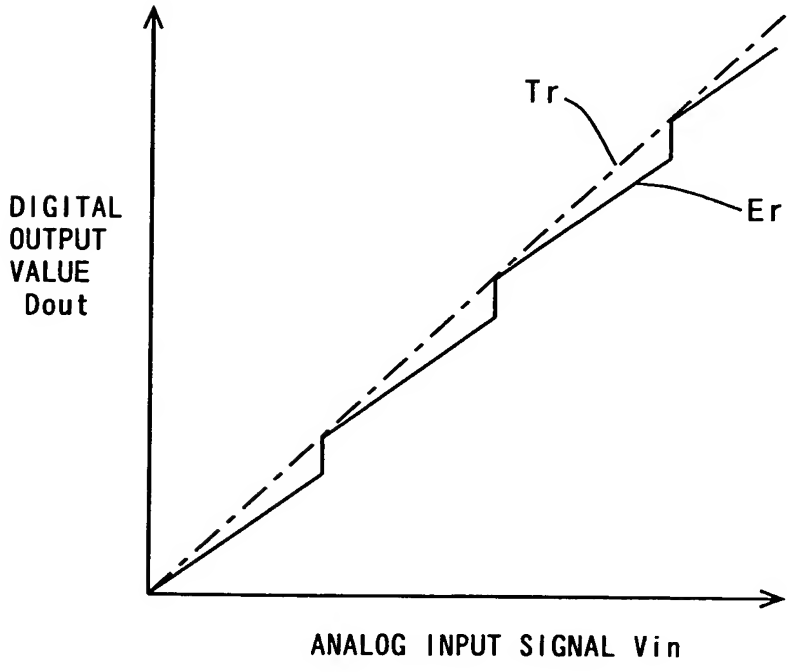


FIG. 5

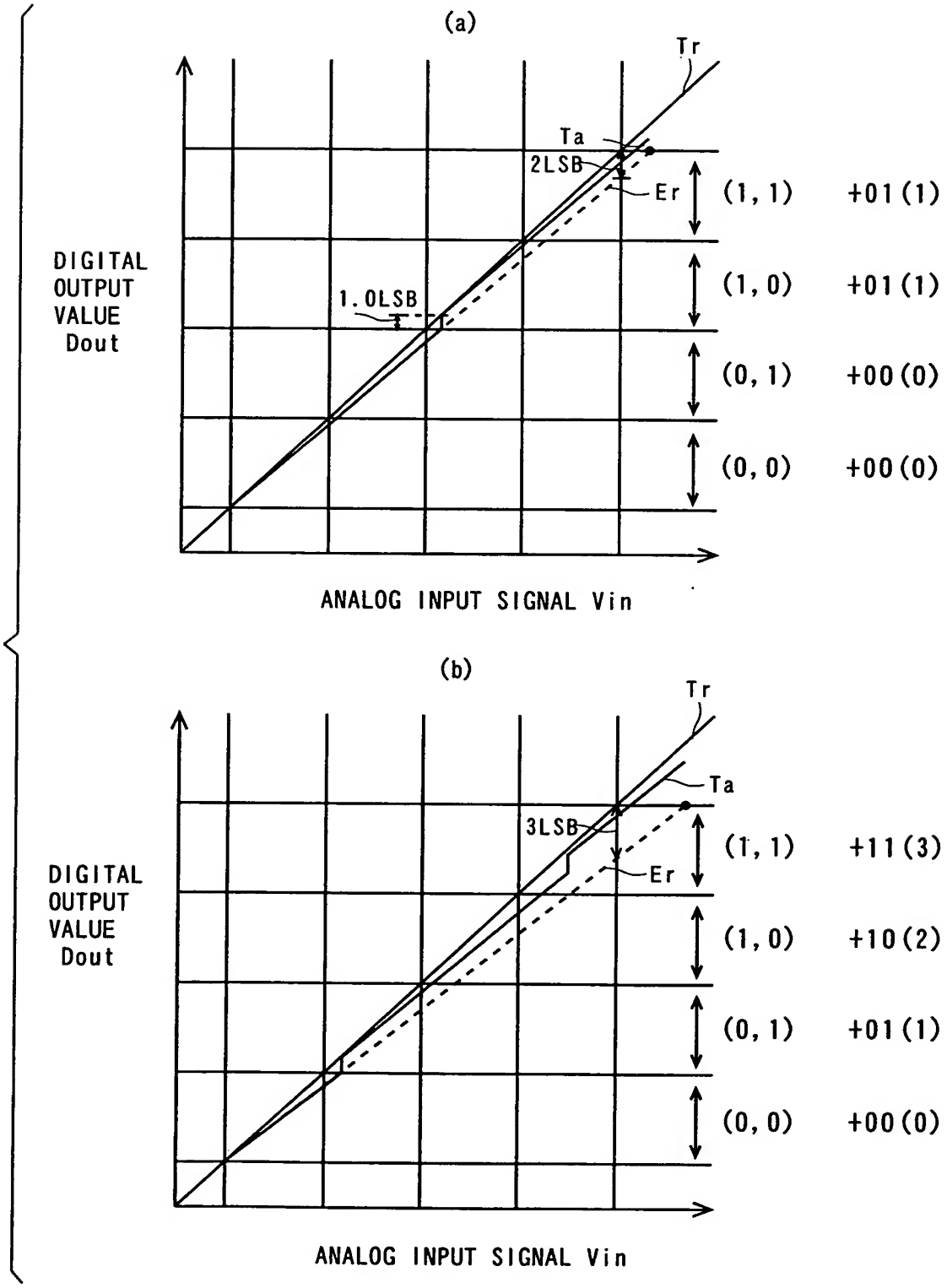

(a)
Tr
Ta
2LSB
Er
1.0LSB
DIGITAL OUTPUT VALUE Dout
(1, 1) +01 (1)
(1, 0) +01 (1)
(0, 1) +00 (0)
(0, 0) +00 (0)
ANALOG INPUT SIGNAL Vin
(b)
Tr
Ta
3LSB
Er
DIGITAL OUTPUT VALUE Dout
(1, 1) +11 (3)
(1, 0) +10 (2)
(0, 1) +01 (1)
(0, 0) +00 (0)
ANALOG INPUT SIGNAL Vin

FIG. 6

TBL

		DC CONTROL SIGNAL IN1, IN2			
D5	D4	0, 0	0, 1	1, 0	1, 1
1	1	000 (0)	001 (1)	010 (2)	100 (4)
1	0	000 (0)	001 (1)	001 (1)	011 (3)
0	1	000 (0)	000 (0)	001 (1)	010 (2)
0	0	000 (0)	000 (0)	000 (0)	000 (0)

FIG. 7

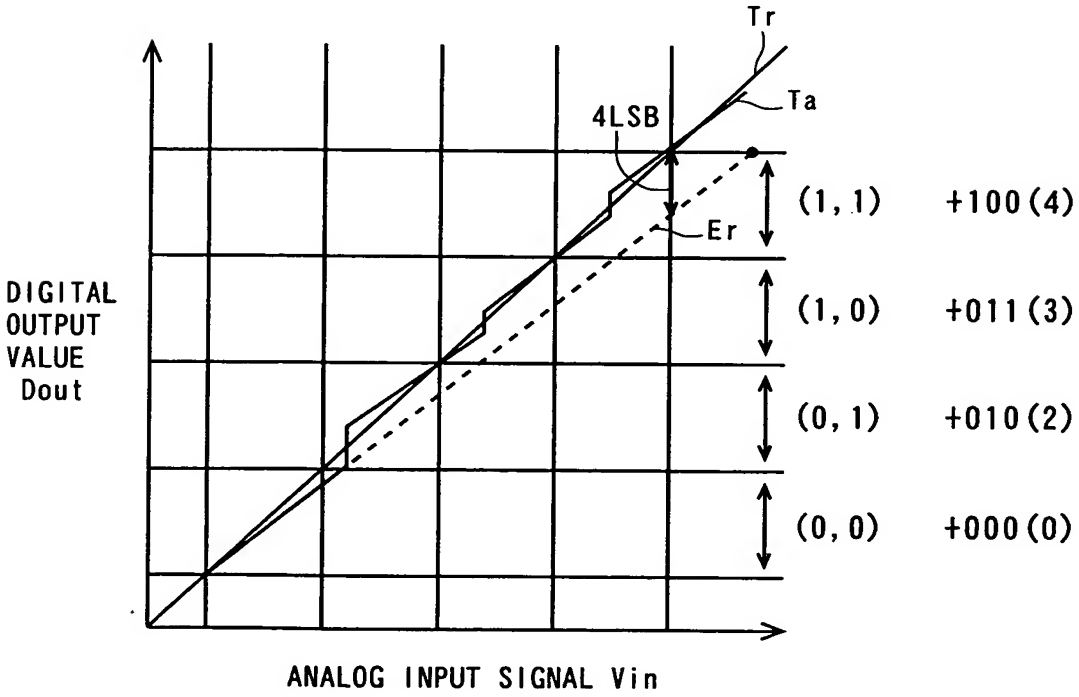


FIG. 8

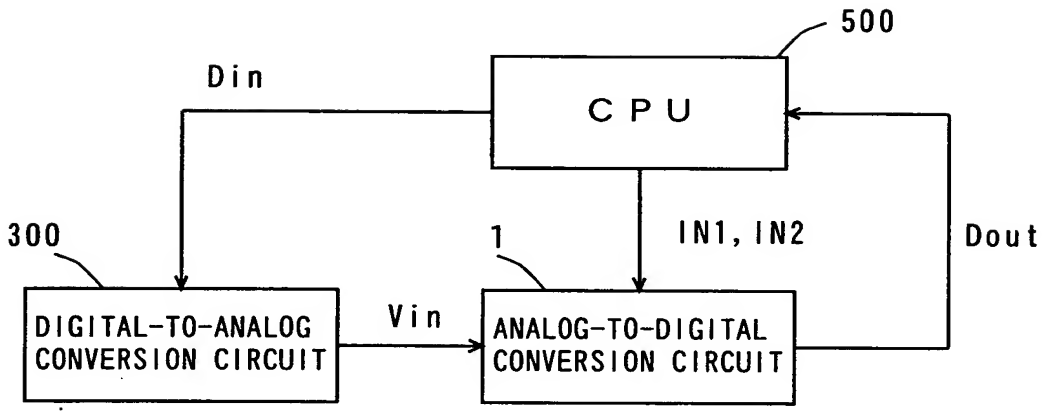

500
CPU
Din
300
1
IN1, IN2
Dout
DIGITAL-TO-ANALOG CONVERSION CIRCUIT
Vin
ANALOG-TO-DIGITAL CONVERSION CIRCUIT

FIG. 9

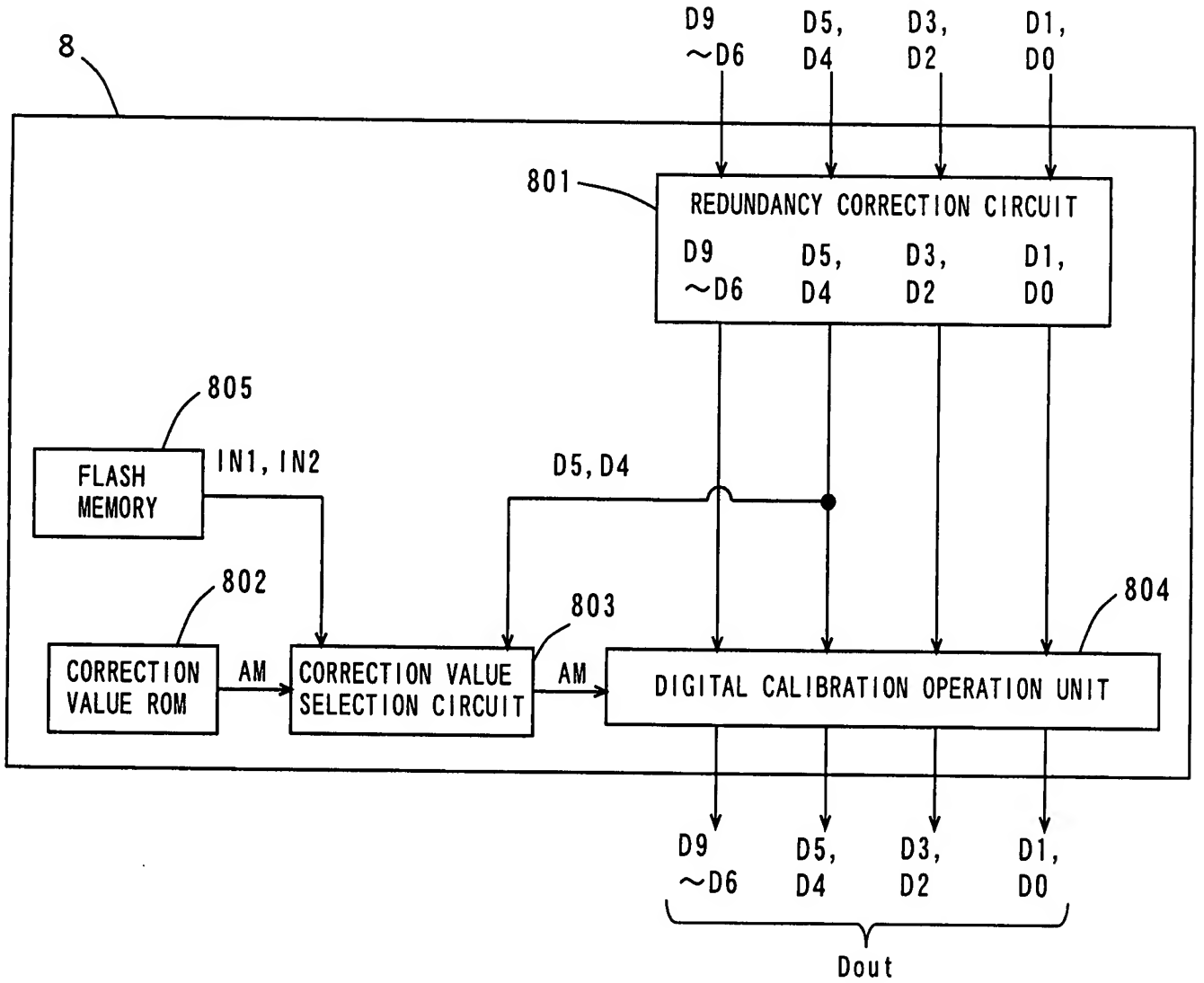

8
D9 ~D6
D5, D4
D3, D2
D1, D0
801
REDUNDANCY CORRECTION CIRCUIT
D9 ~D6
D5, D4
D3, D2
D1, D0
805
FLASH MEMORY
IN1, IN2
D5, D4
802
CORRECTION VALUE ROM
AM
803
CORRECTION VALUE SELECTION CIRCUIT
AM
804
DIGITAL CALIBRATION OPERATION UNIT
D9 ~D6
D5, D4
D3, D2
D1, D0
Dout

FIG. 10

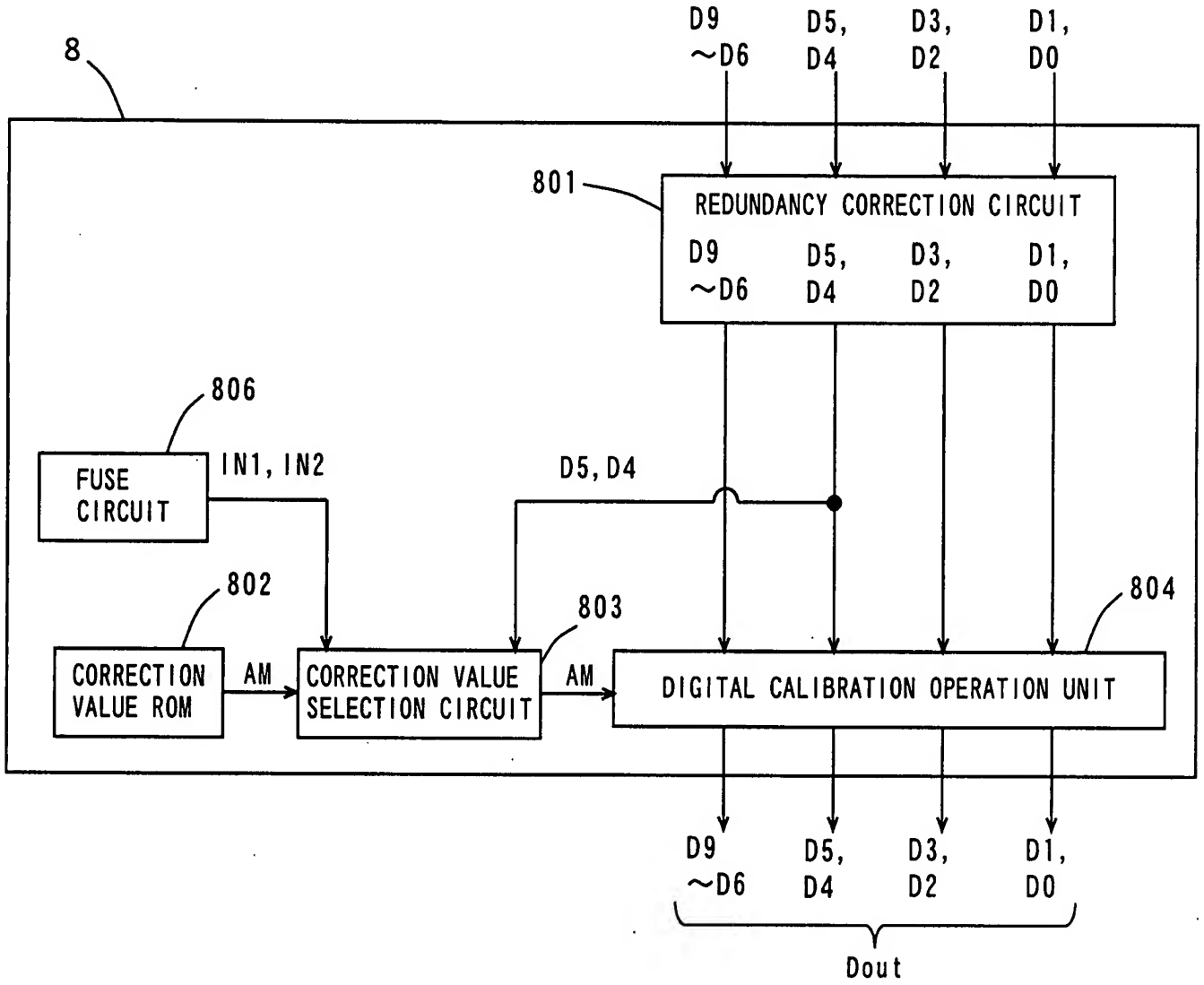

8
D9 ~D6
D5, D4
D3, D2
D1, D0
801
REDUNDANCY CORRECTION CIRCUIT
D9 ~D6
D5, D4
D3, D2
D1, D0
806
FUSE CIRCUIT
IN1, IN2
D5, D4
802
CORRECTION VALUE ROM
AM
803
CORRECTION VALUE SELECTION CIRCUIT
AM
804
DIGITAL CALIBRATION OPERATION UNIT
D9 ~D6
D5, D4
D3, D2
D1, D0
Dout

FIG. 11

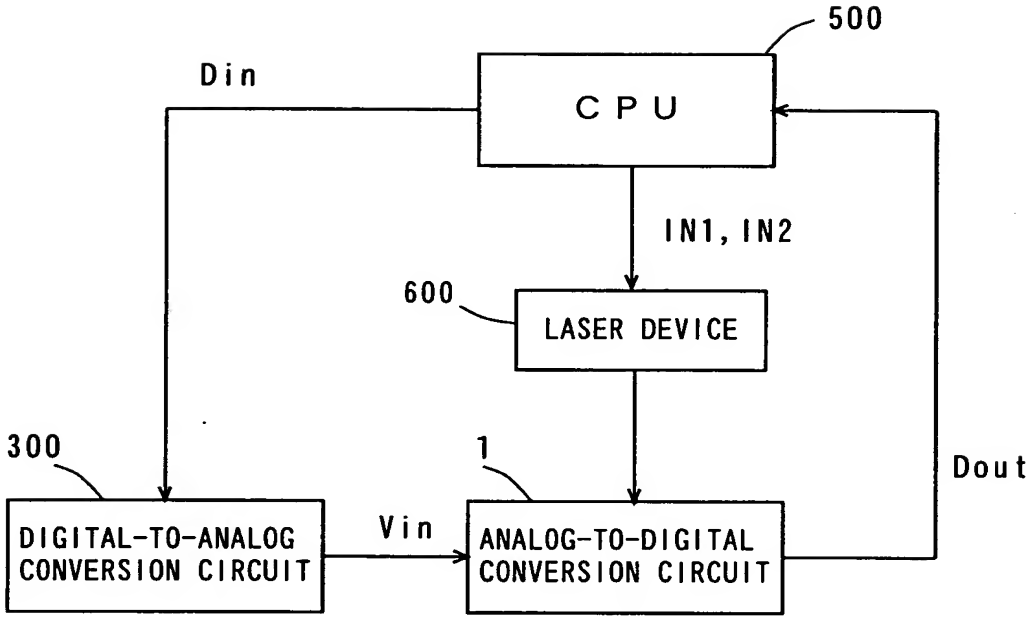

500
CPU
Din
IN1, IN2
600
LASER DEVICE
300
1
Dout
DIGITAL-TO-ANALOG CONVERSION CIRCUIT
Vin
ANALOG-TO-DIGITAL CONVERSION CIRCUIT

FIG. 12

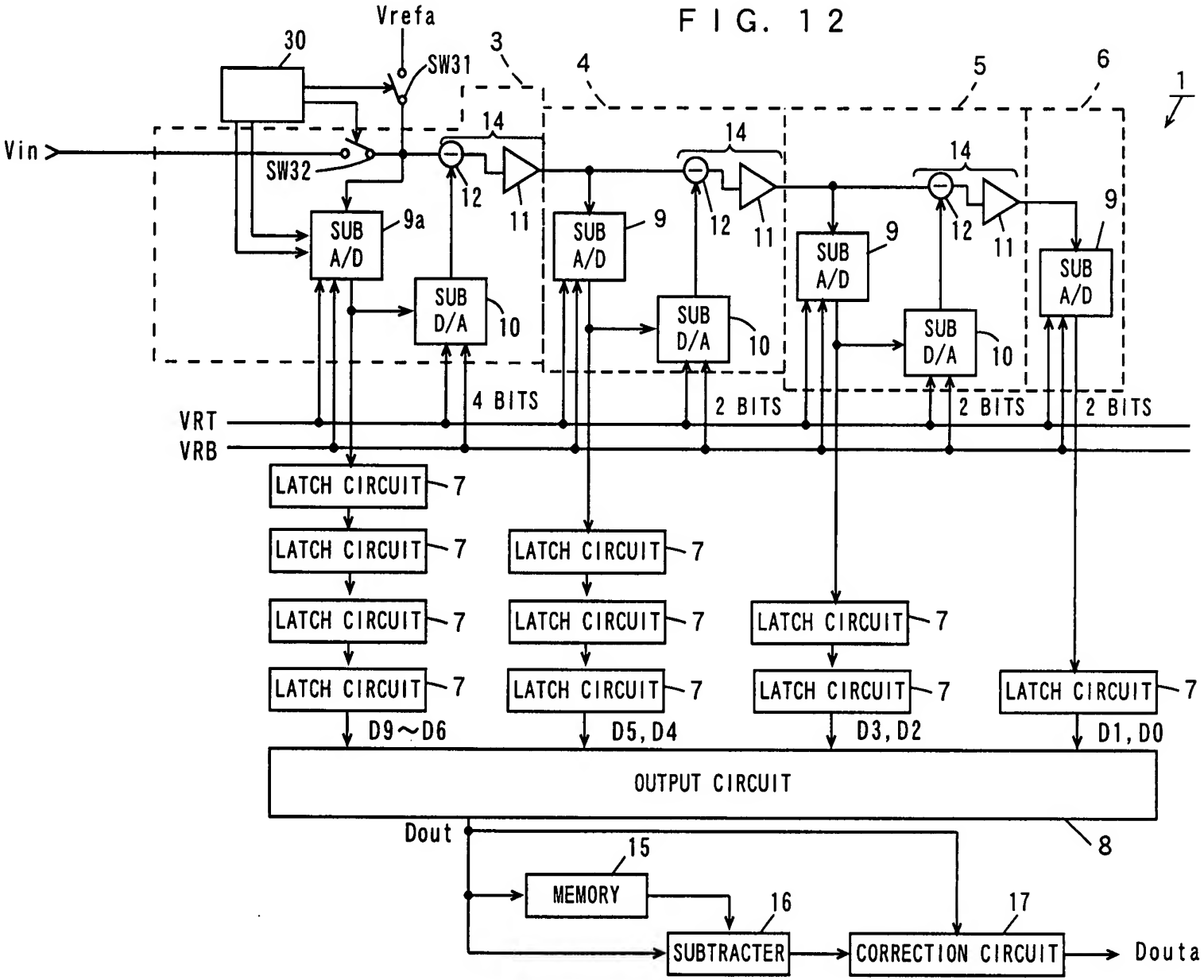

Vrefa
30
SW31
3
4
5
6
1
Vin
SW32
14
12
11
SUB A/D
9a
9
SUB D/A
10
4 BITS
2 BITS
VRT
VRB
LATCH CIRCUIT
7
D9~D6
D5, D4
D3, D2
D1, D0
OUTPUT CIRCUIT
8
Dout
15
MEMORY
16
SUBTRACTER
17
CORRECTION CIRCUIT
Douta

FIG. 13

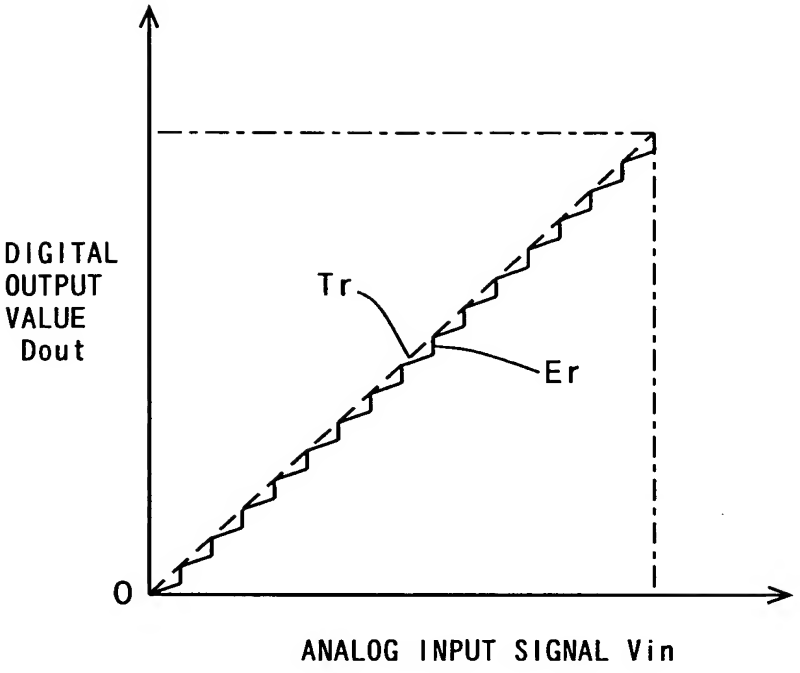

DIGITAL
OUTPUT
VALUE
Dout
Tr
Er
0
ANALOG INPUT SIGNAL Vin

FIG. 14

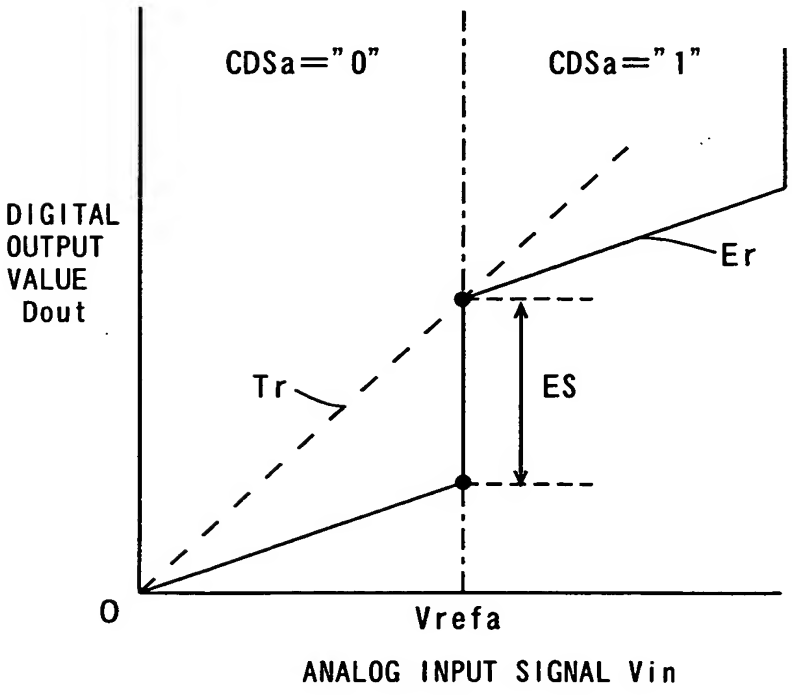

CDSa="0"
CDSa="1"
DIGITAL
OUTPUT
VALUE
Dout
Er
Tr
ES
0
Vrefa
ANALOG INPUT SIGNAL Vin

FIG. 15

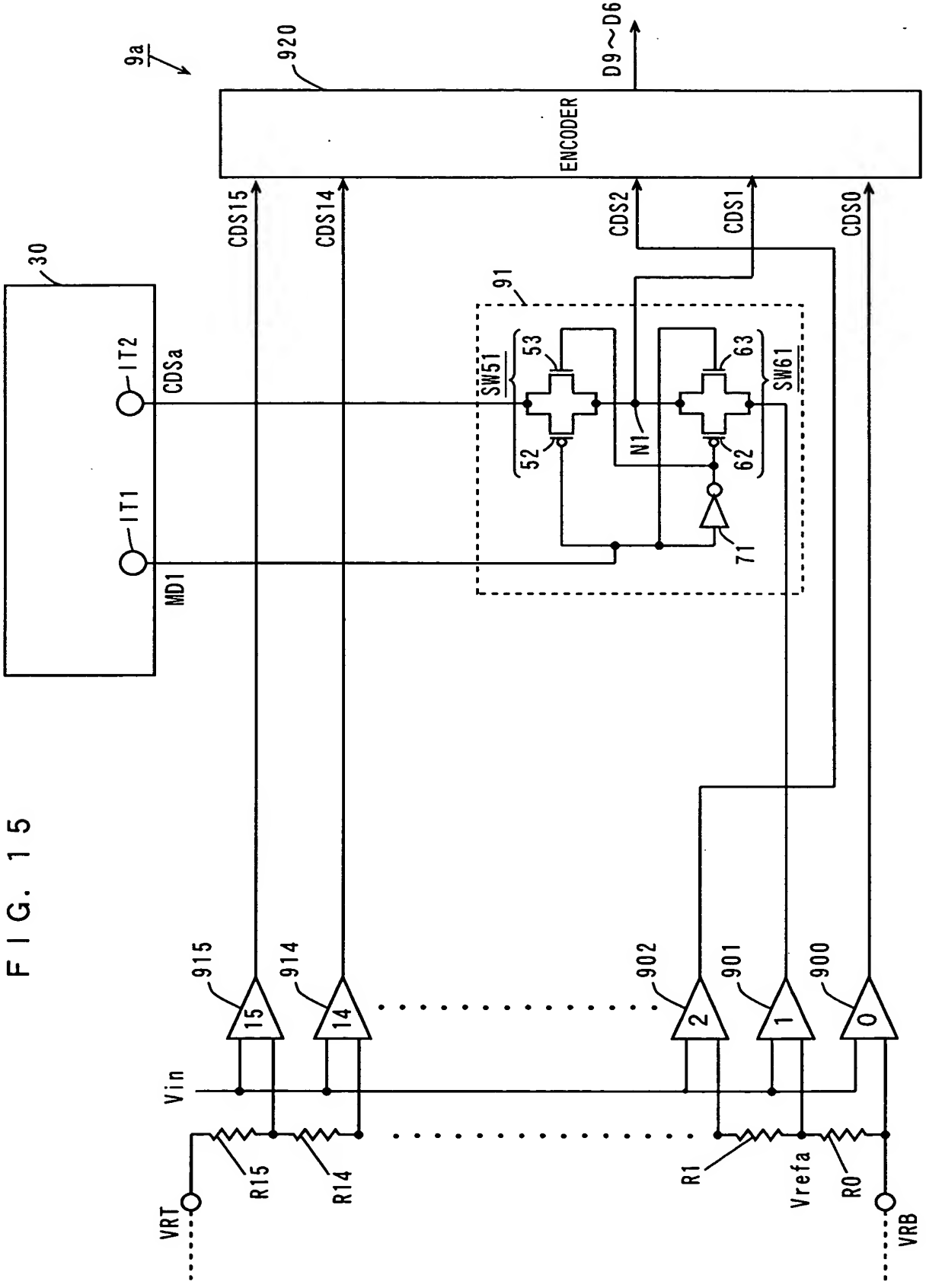

9a
920
ENCODER
D9～D6
30
IT2
CDSa
IT1
MD1
CDS15
CDS14
CDS2
CDS1
CDS0
91
SW51
53
52
N1
63
62
SW61
71
915
914
902
901
900
15
14
2
1
0
Vin
R15
R14
R1
Vrefa
R0
VRT
VRB

FIG. 16

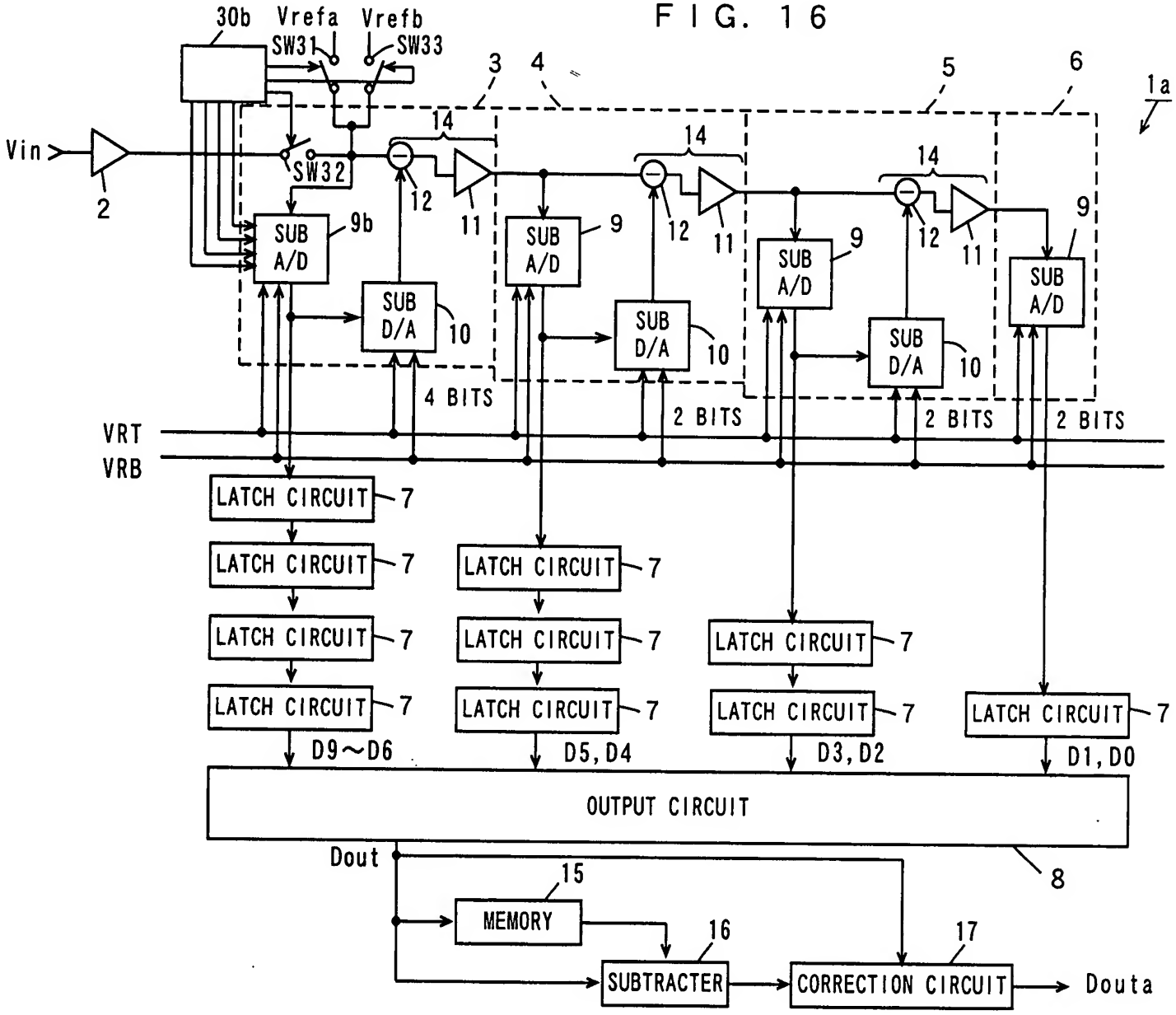

30b
Vrefa
Vrefb
SW31
SW33
SW32
Vin
2
3
4
5
6
1a
14
12
11
9
9b
SUB A/D
SUB D/A
10
4 BITS
2 BITS
VRT
VRB
LATCH CIRCUIT
7
D9～D6
D5, D4
D3, D2
D1, D0
OUTPUT CIRCUIT
8
Dout
15
MEMORY
16
SUBTRACTER
17
CORRECTION CIRCUIT
Douta

FIG. 17

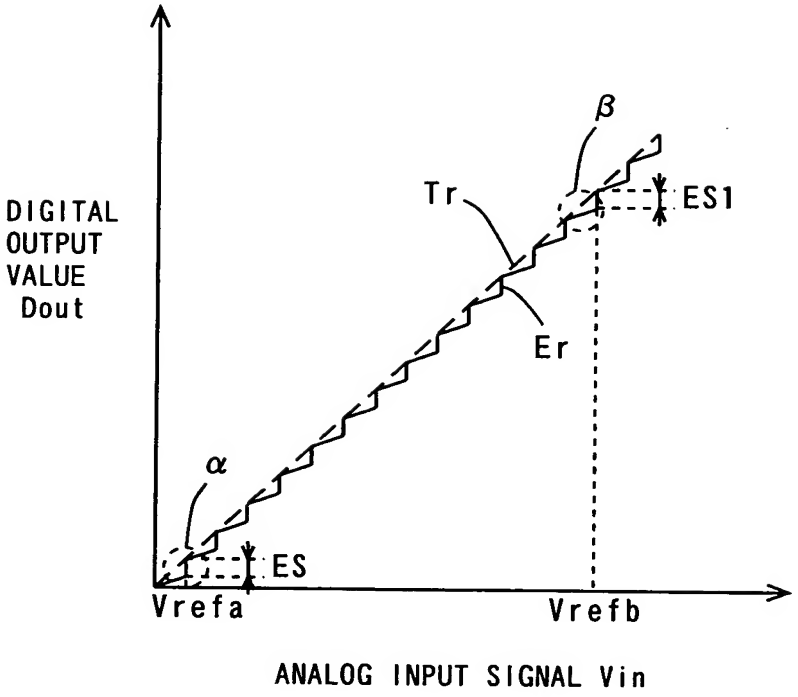

DIGITAL
OUTPUT
VALUE
Dout
β
Tr
ES1
Er
α
ES
Vrefa
Vrefb
ANALOG INPUT SIGNAL Vin

FIG. 18

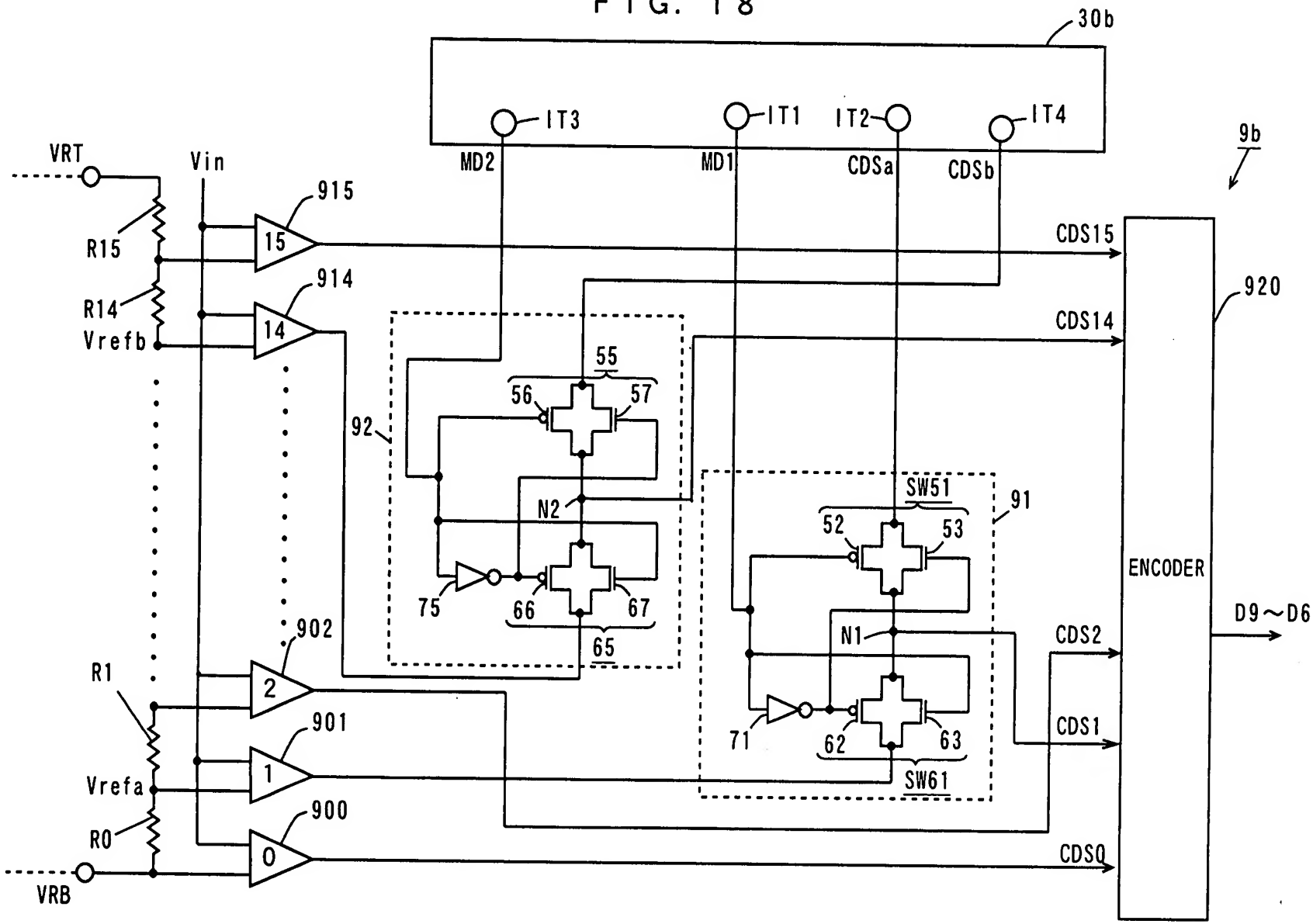

30b
IT3
IT1
IT2
IT4
MD2
MD1
CDSa
CDSb
9b
VRT
Vin
915
R15
15
CDS15
914
R14
14
CDS14
Vrefb
920
55
56
57
92
N2
SW51
91
52
53
ENCODER
D9～D6
75
66
67
65
902
CDS2
R1
2
N1
901
CDS1
1
71
62
63
SW61
Vrefa
900
R0
0
CDS0
VRB

FIG. 19

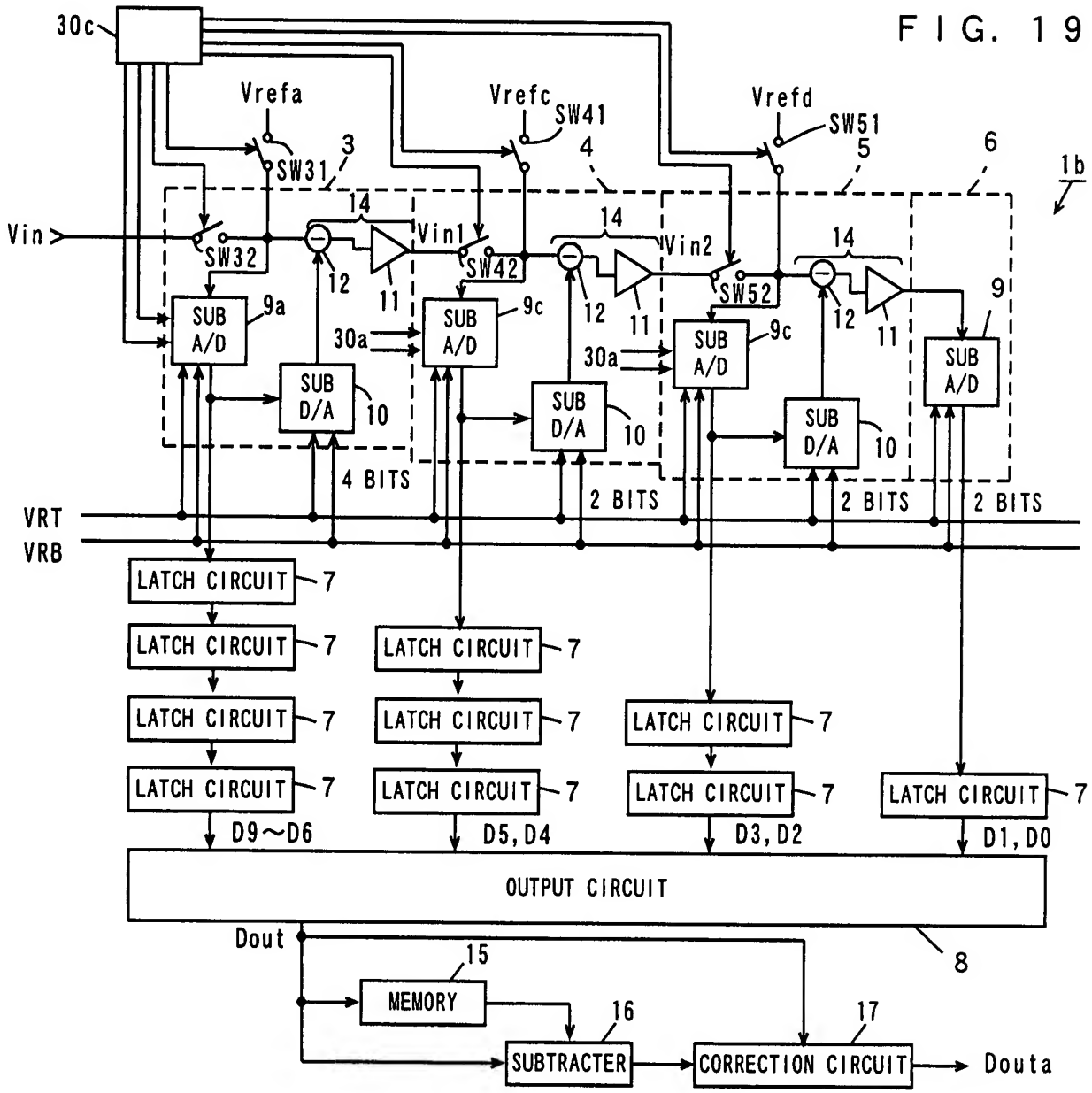
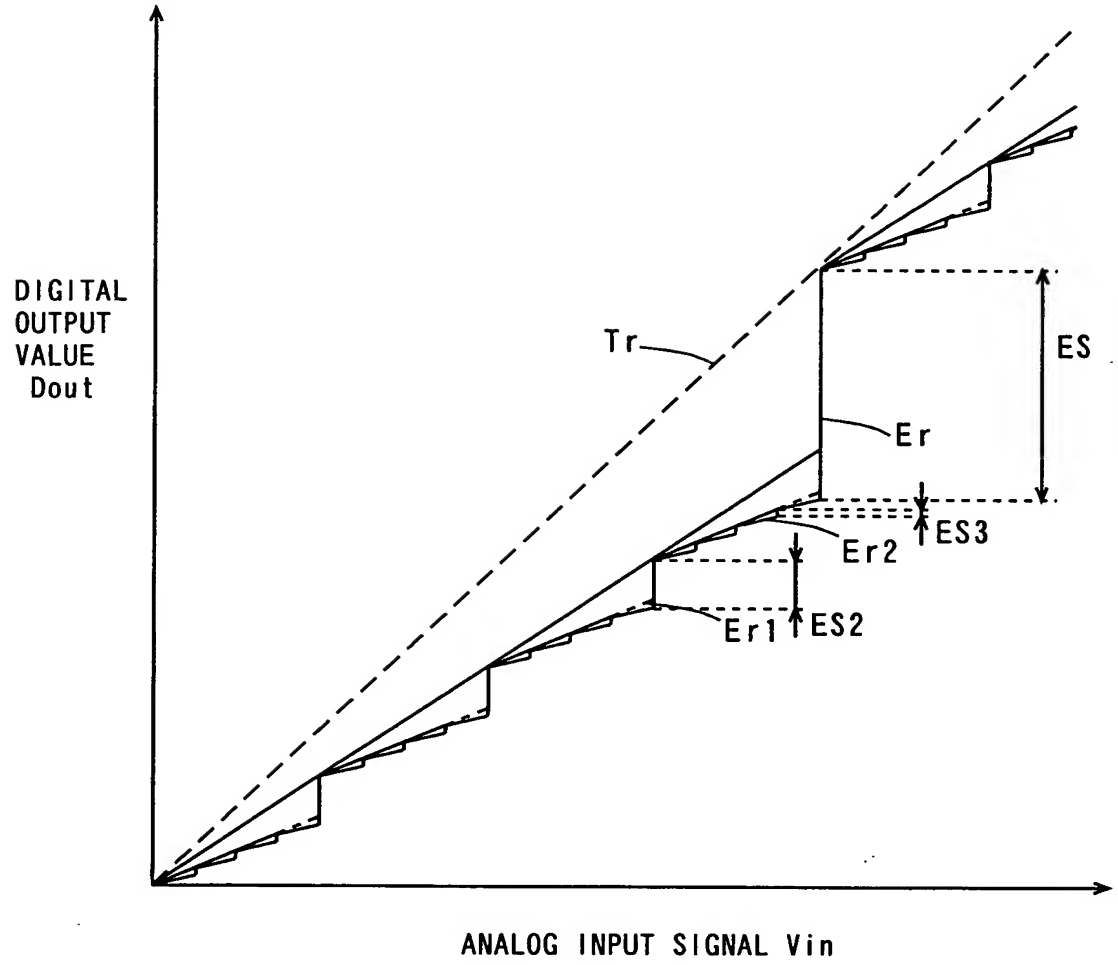

30c
Vrefa
Vrefc
Vrefd
SW31
SW41
SW51
3
4
5
6
1b
Vin
Vin1
Vin2
SW32
SW42
SW52
14
12
11
9
SUB A/D
9a
9c
SUB D/A
10
30a
4 BITS
2 BITS
VRT
VRB
LATCH CIRCUIT
7
D9~D6
D5, D4
D3, D2
D1, D0
OUTPUT CIRCUIT
8
Dout
15
MEMORY
16
SUBTRACTER
17
CORRECTION CIRCUIT
Douta

FIG. 20


DIGITAL
OUTPUT
VALUE
Dout
Tr
ES
Er
ES3
Er2
Er1
ES2
ANALOG INPUT SIGNAL Vin

F I G. 2 1

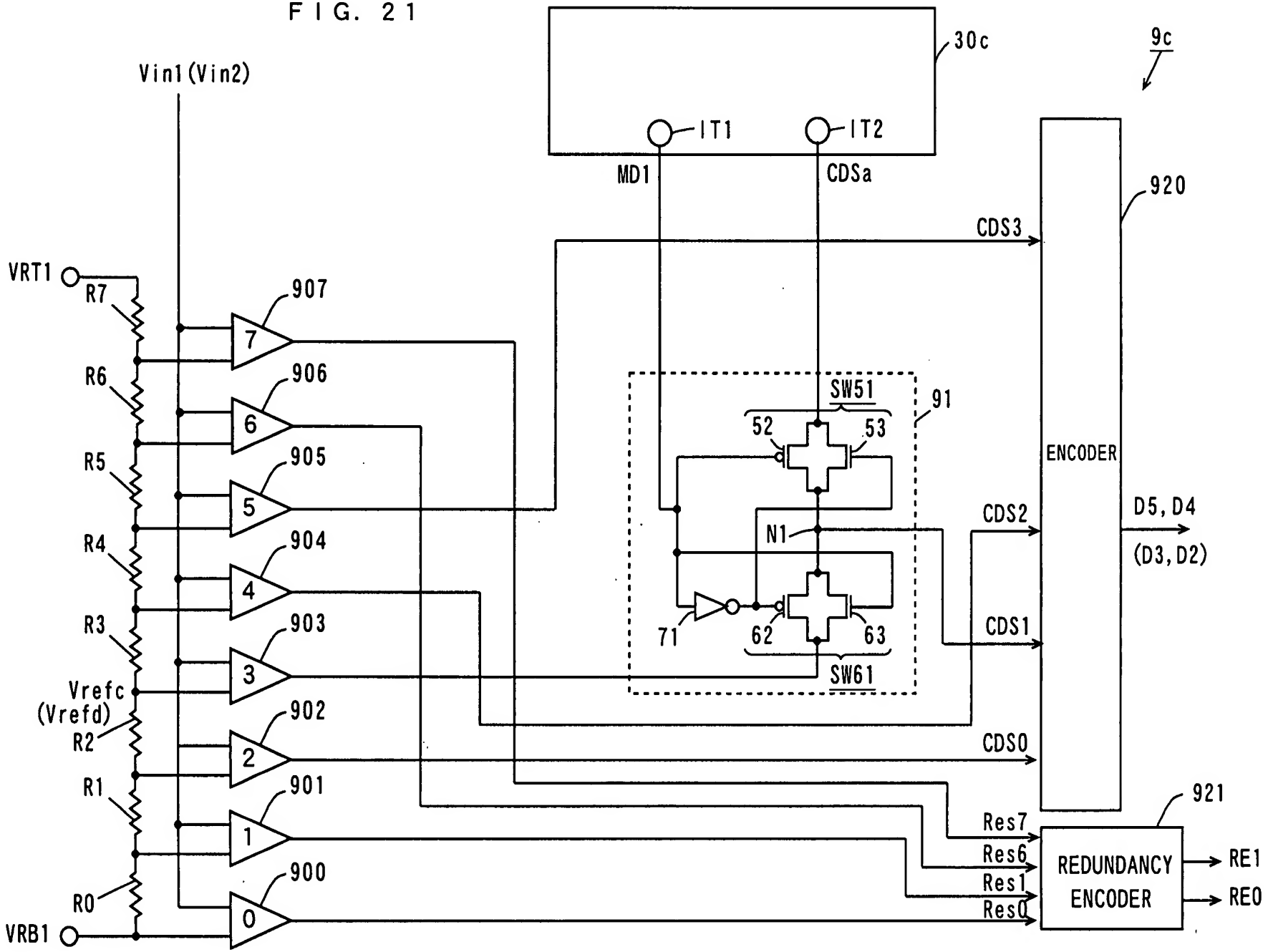

30c
9c
Vin1(Vin2)
IT1
IT2
MD1
CDSa
920
CDS3
VRT1
R7
907
R6
906
R5
905
R4
904
R3
903
Vrefc
(Vrefd)
R2
902
R1
901
R0
900
VRB1
SW51
91
52
53
N1
71
62
63
SW61
ENCODER
CDS2
D5, D4
(D3, D2)
CDS1
CDS0
921
Res7
Res6
Res1
Res0
REDUNDANCY
ENCODER
RE1
RE0

FIG. 22

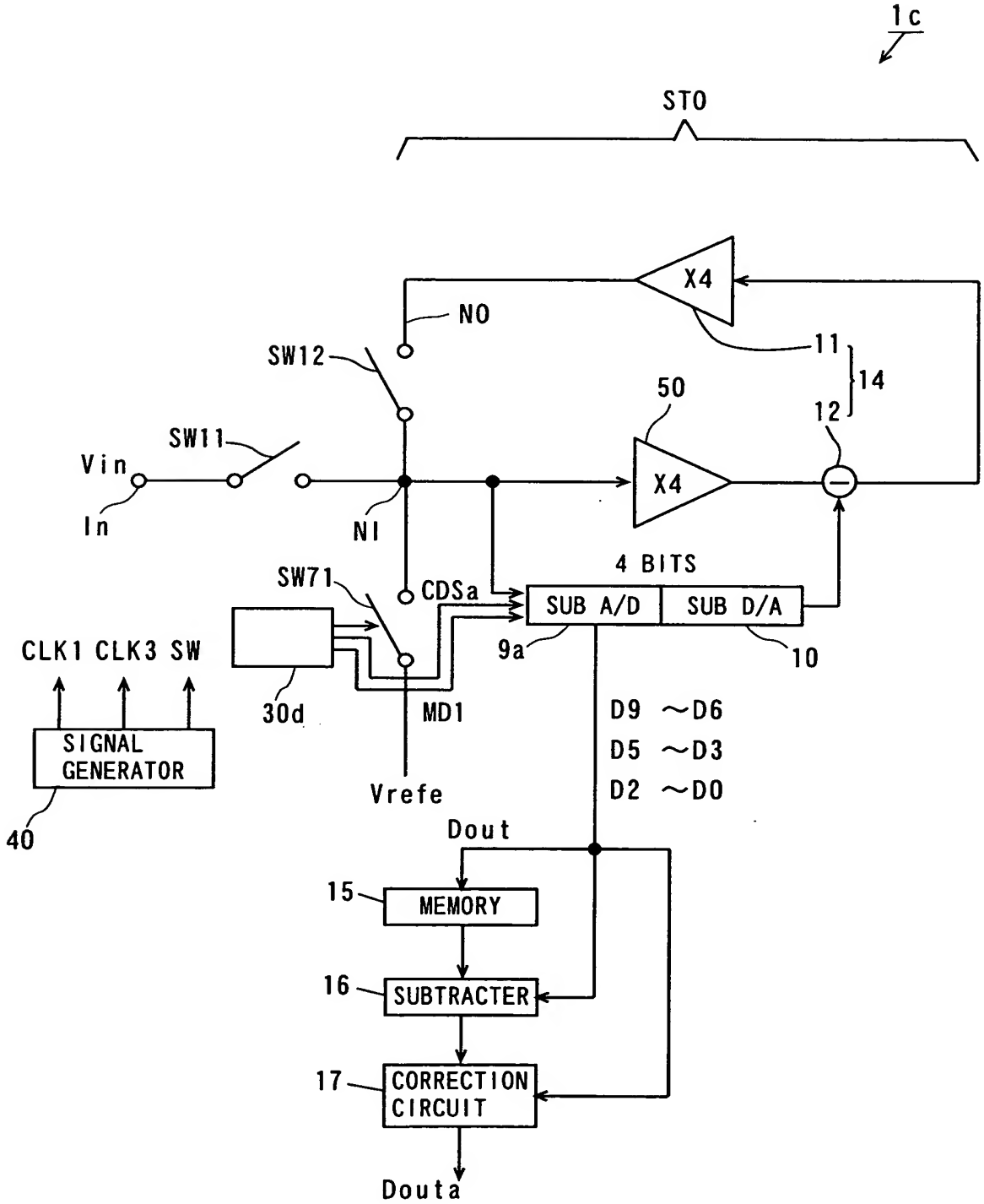

1c
STO
X4
NO
11
14
SW12
50
12
SW11
Vin
X4
In
NI
4 BITS
SW71
CDSa
SUB A/D
SUB D/A
CLK1 CLK3 SW
9a
10
30d
MD1
D9 ~D6
D5 ~D3
D2 ~D0
SIGNAL GENERATOR
Vrefe
40
Dout
15
MEMORY
16
SUBTRACTER
17
CORRECTION CIRCUIT
Douta

FIG. 23

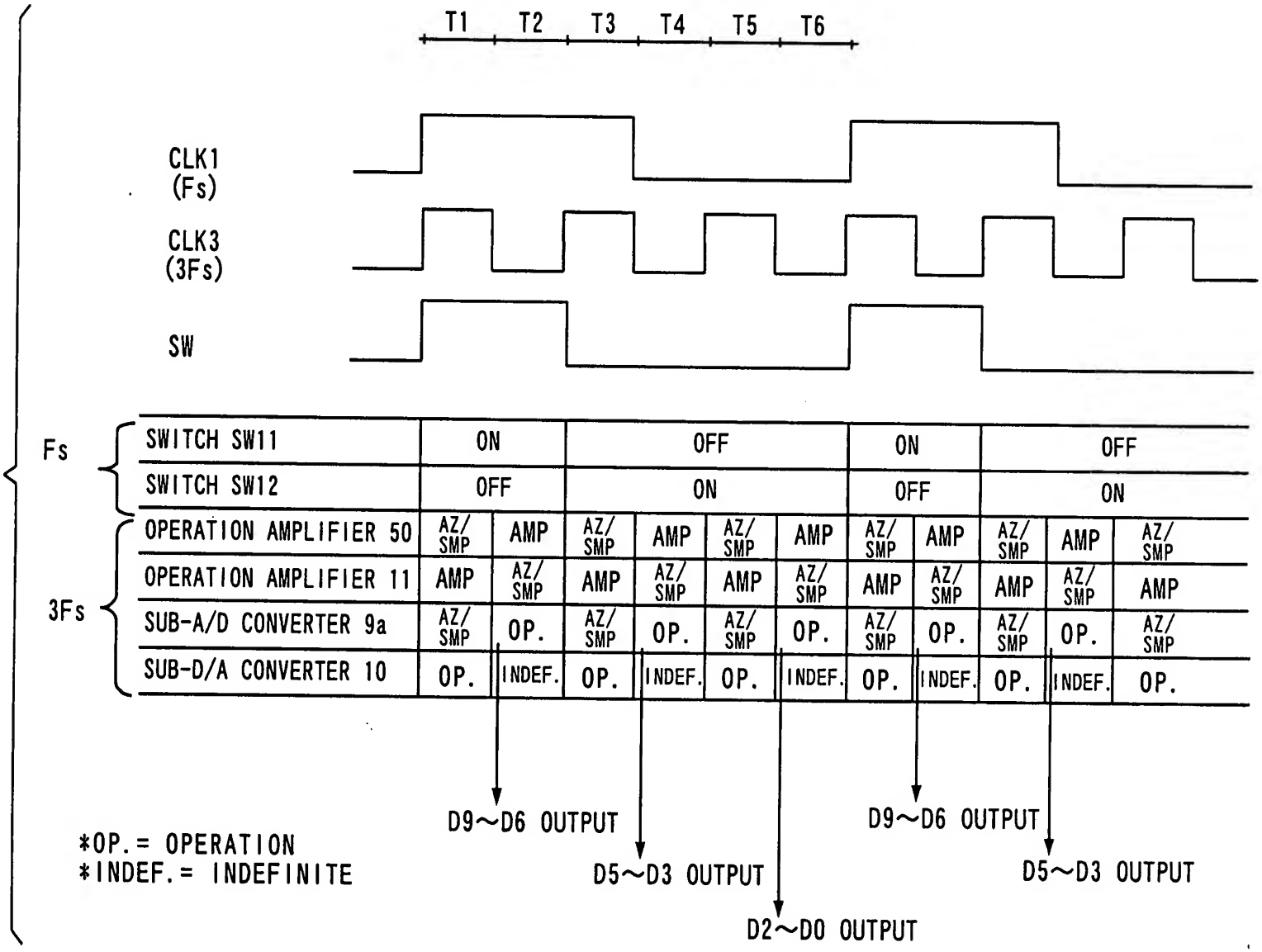

T1
T2
T3
T4
T5
T6
CLK1
(Fs)
CLK3
(3Fs)
SW
Fs
3Fs
SWITCH SW11
SWITCH SW12
OPERATION AMPLIFIER 50
OPERATION AMPLIFIER 11
SUB-A/D CONVERTER 9a
SUB-D/A CONVERTER 10
ON
OFF
AZ/SMP
AMP
OP.
INDEF.
D9～D6 OUTPUT
D5～D3 OUTPUT
D2～D0 OUTPUT
*OP.= OPERATION
*INDEF.= INDEFINITE

FIG. 24

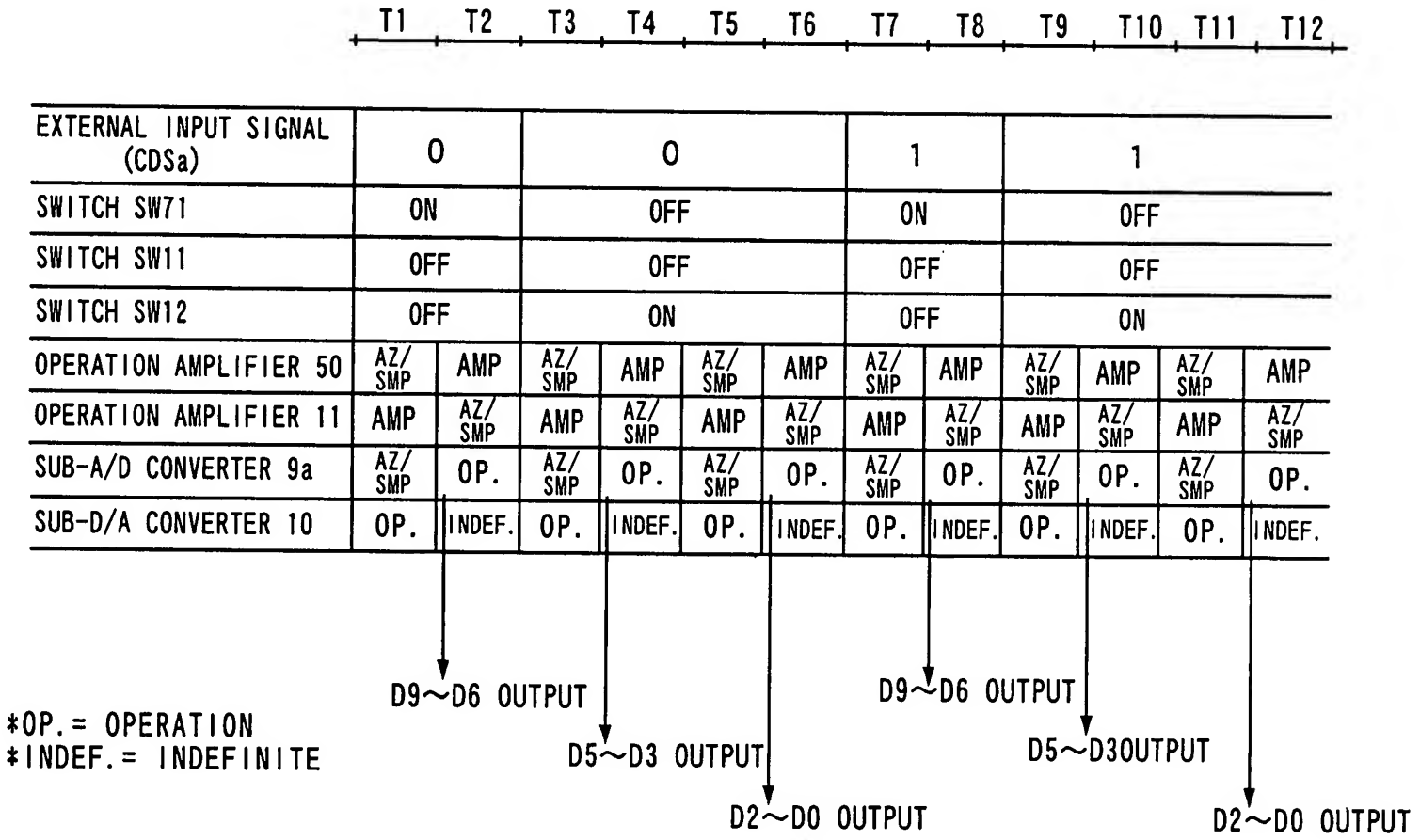

T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12
EXTERNAL INPUT SIGNAL (CDSa)
0
0
1
1
SWITCH SW71
ON
OFF
ON
OFF
SWITCH SW11
OFF
OFF
OFF
OFF
SWITCH SW12
OFF
ON
OFF
ON
OPERATION AMPLIFIER 50
AZ/SMP
AMP
OPERATION AMPLIFIER 11
AMP
AZ/SMP
SUB-A/D CONVERTER 9a
AZ/SMP
OP.
SUB-D/A CONVERTER 10
OP.
INDEF.
D9~D6 OUTPUT
D5~D3 OUTPUT
D2~D0 OUTPUT
D9~D6 OUTPUT
D5~D3OUTPUT
D2~D0 OUTPUT
*OP.= OPERATION
*INDEF.= INDEFINITE

FIG. 25

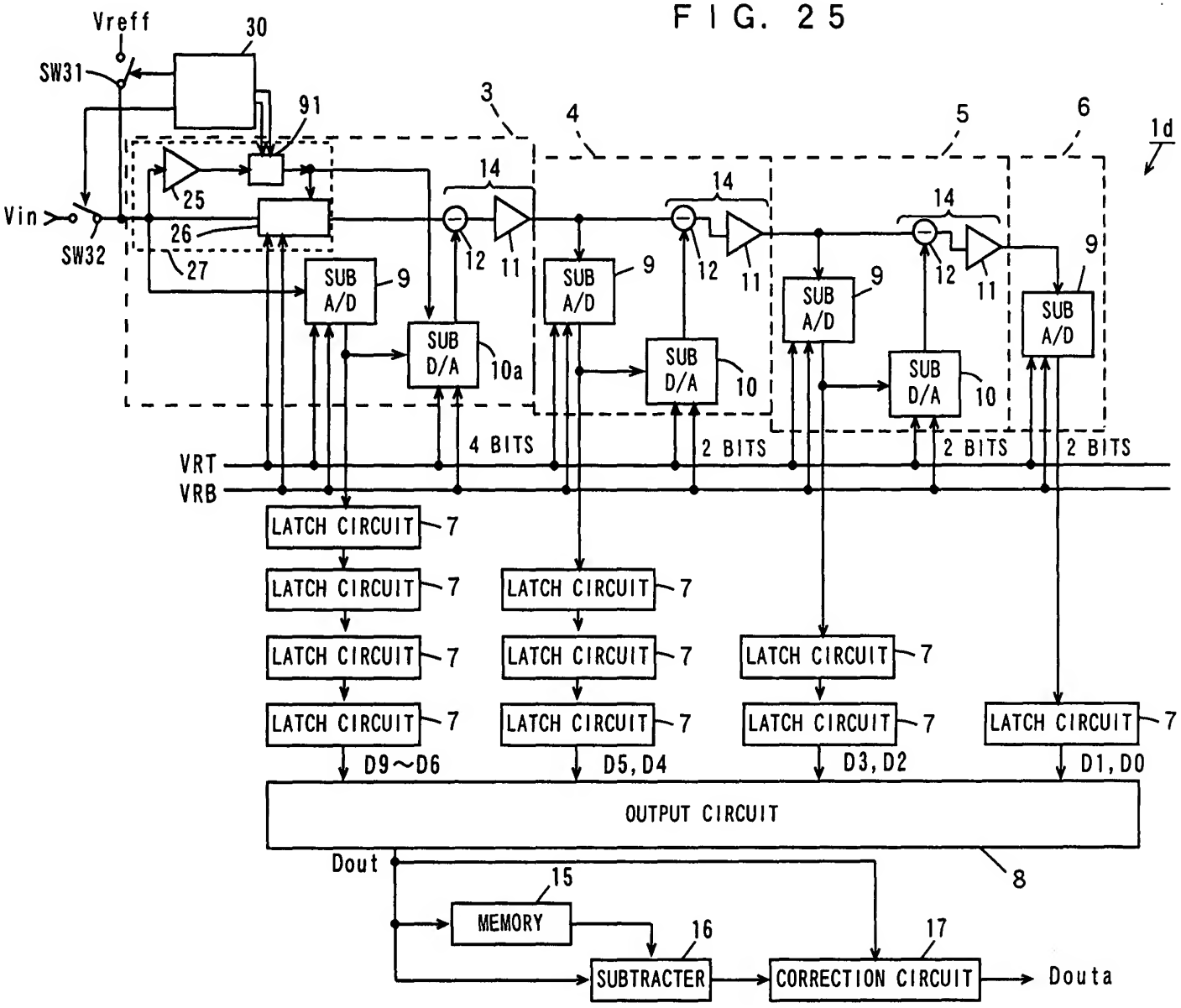

Vreff
30
SW31
91
3
4
5
6
1d
Vin
SW32
25
26
27
14
12
11
SUB A/D
9
SUB D/A
10a
10
4 BITS
2 BITS
VRT
VRB
LATCH CIRCUIT
7
D9~D6
D5, D4
D3, D2
D1, D0
OUTPUT CIRCUIT
8
Dout
15
MEMORY
16
SUBTRACTER
17
CORRECTION CIRCUIT
Douta

FIG. 26

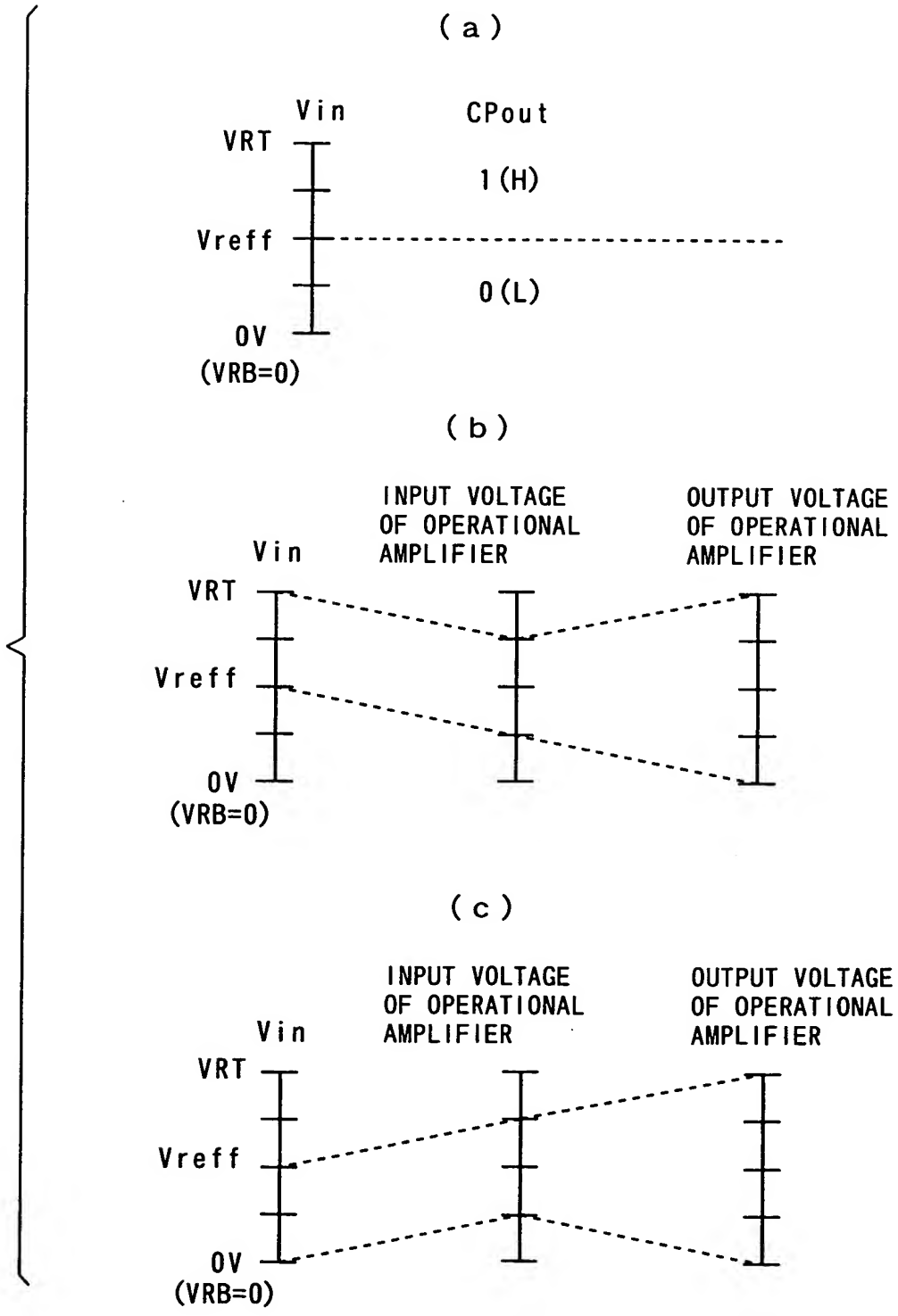

(a)
Vin
CPout
VRT
1(H)
Vreff
0(L)
0V
(VRB=0)
(b)
INPUT VOLTAGE OF OPERATIONAL AMPLIFIER
OUTPUT VOLTAGE OF OPERATIONAL AMPLIFIER
Vin
VRT
Vreff
0V
(VRB=0)
(c)
INPUT VOLTAGE OF OPERATIONAL AMPLIFIER
OUTPUT VOLTAGE OF OPERATIONAL AMPLIFIER
Vin
VRT
Vreff
0V
(VRB=0)

FIG. 27

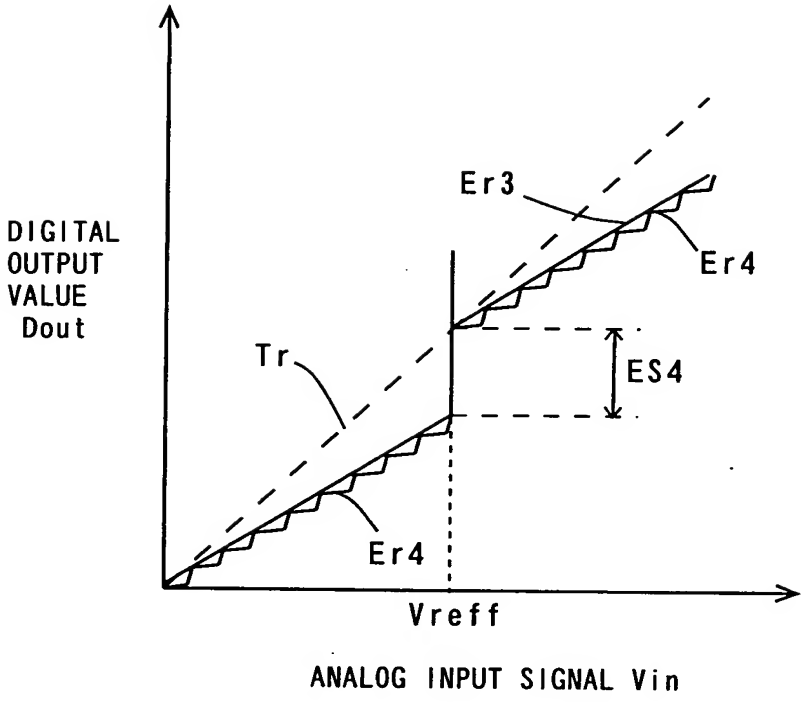

DIGITAL
OUTPUT
VALUE
Dout
Er3
Er4
Tr
ES4
Er4
Vreff
ANALOG INPUT SIGNAL Vin

FIG. 28

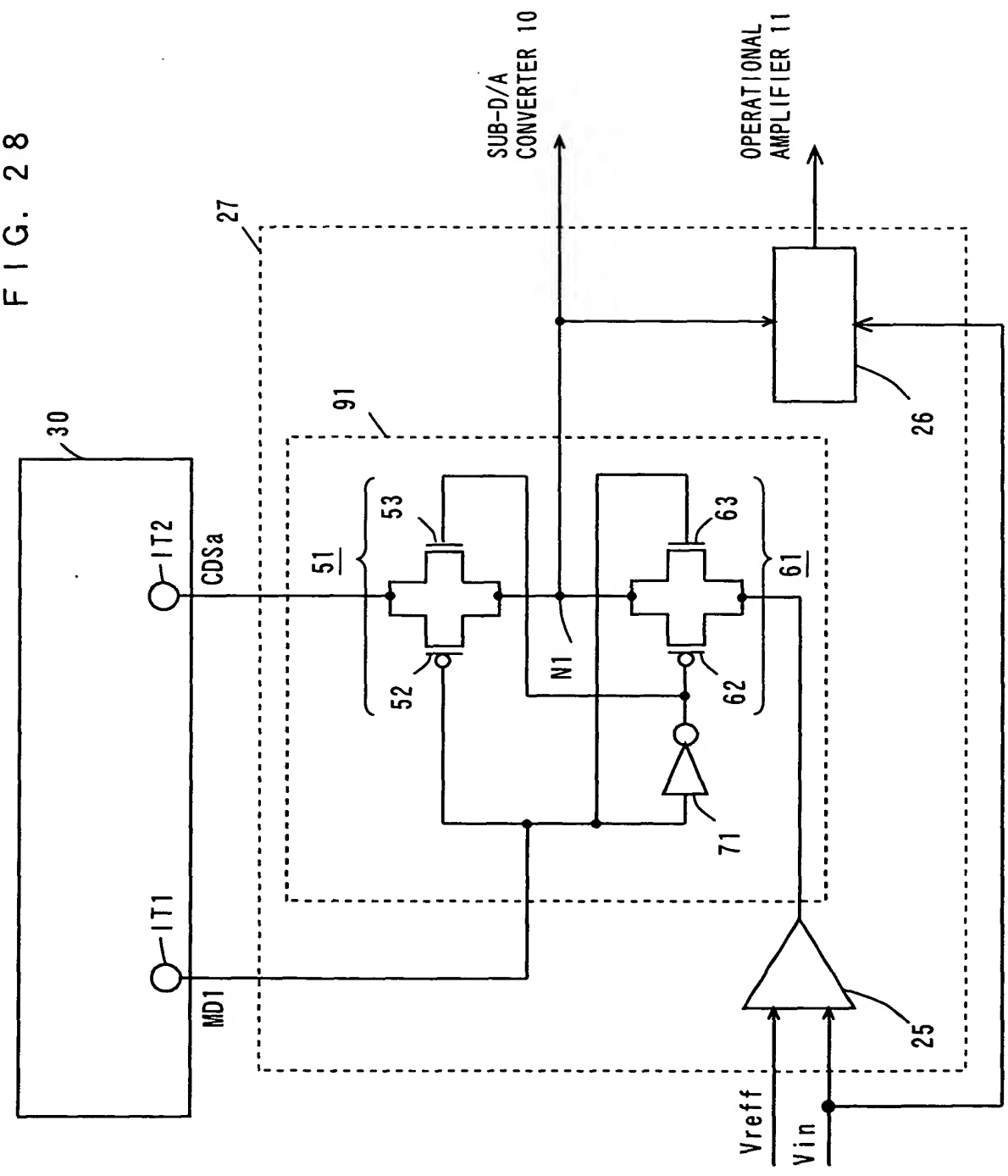

SUB-D/A CONVERTER 10
OPERATIONAL AMPLIFIER 11
27
91
30
IT2
CDSa
IT1
MD1
51
53
52
N1
63
61
62
71
26
25
Vreff
Vin

FIG. 29

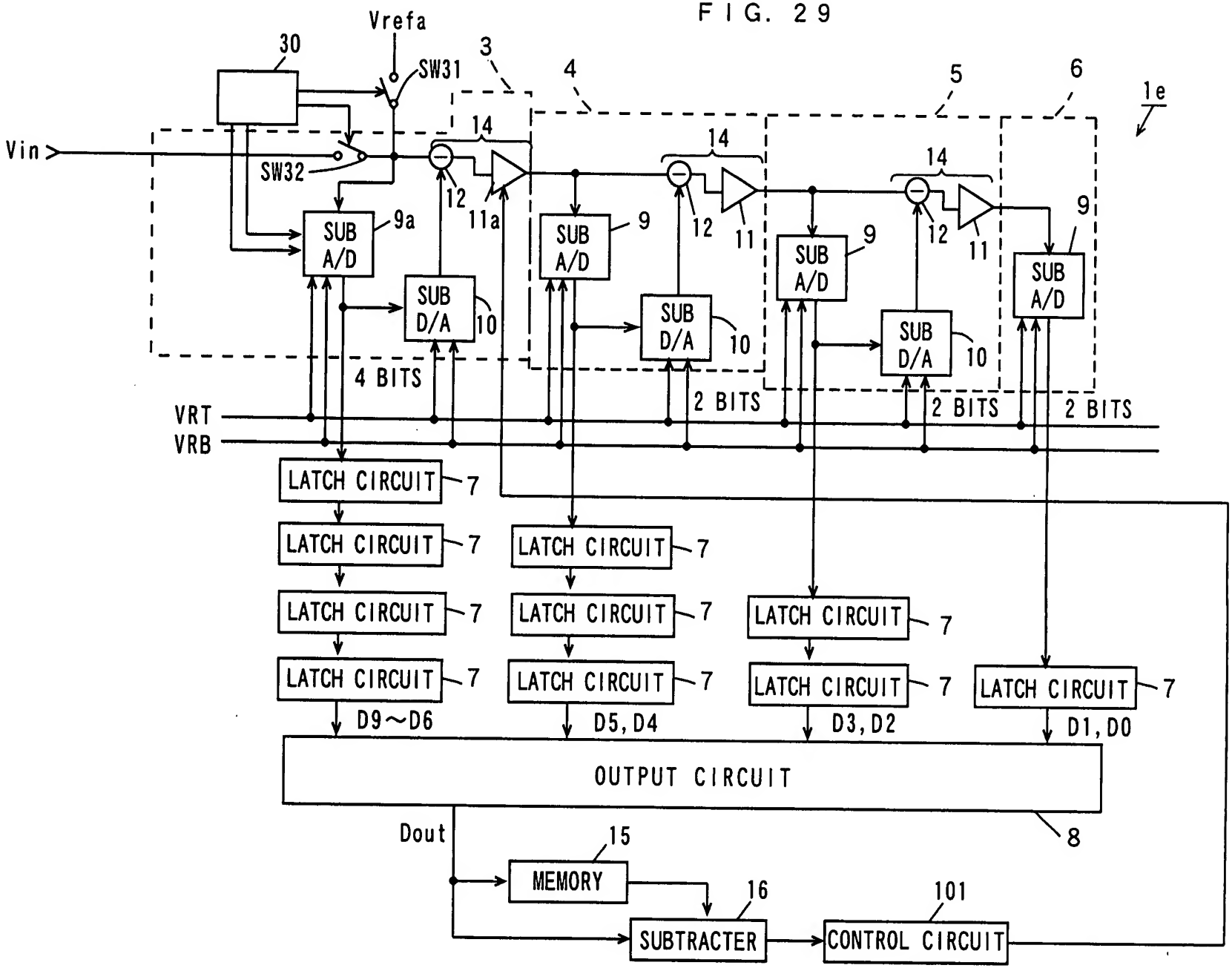

Vrefa
30
SW31
3
4
5
6
1e
Vin
SW32
14
12
11a
11
SUB A/D
9a
9
SUB D/A
10
4 BITS
2 BITS
VRT
VRB
LATCH CIRCUIT
7
D9~D6
D5, D4
D3, D2
D1, D0
OUTPUT CIRCUIT
8
Dout
15
MEMORY
16
SUBTRACTER
101
CONTROL CIRCUIT

FIG. 30

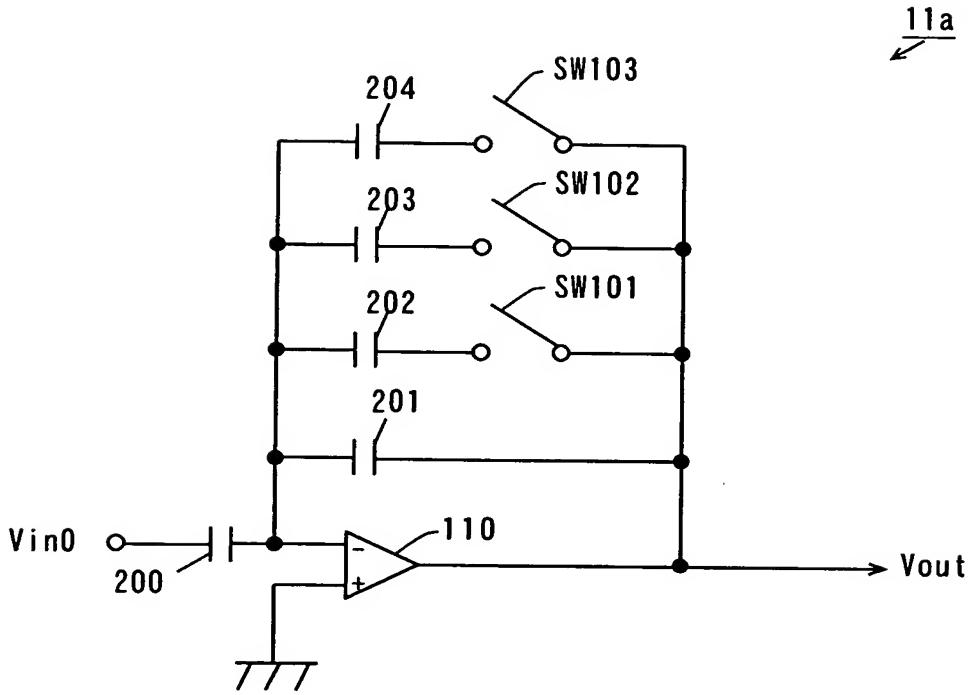
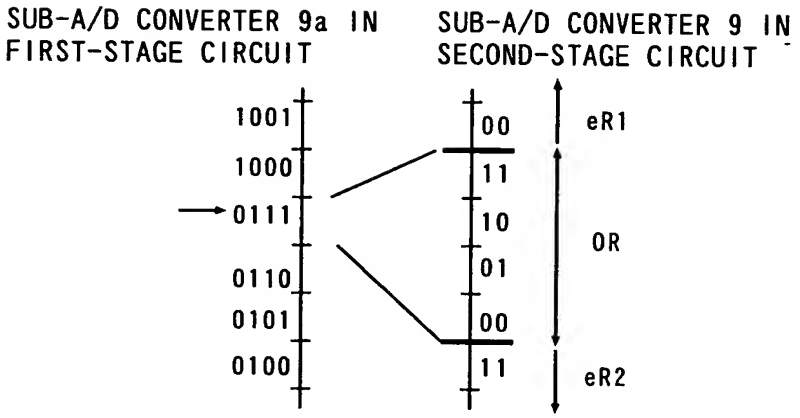
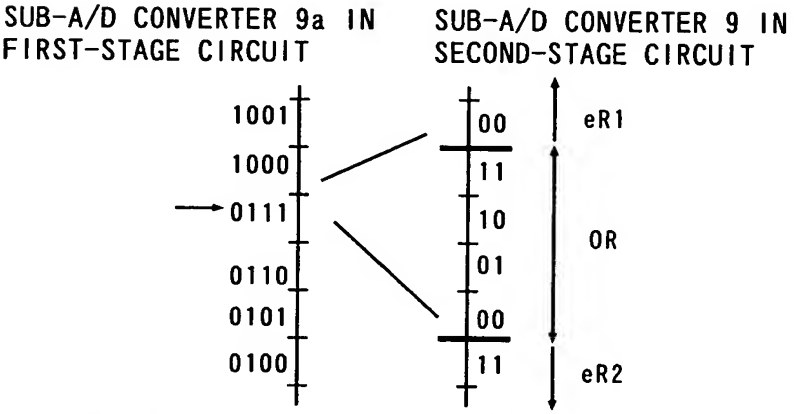


FIG. 31

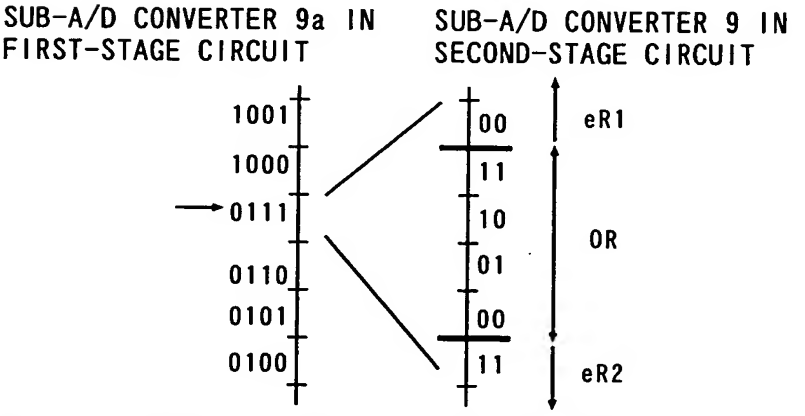
(a)


SUB-A/D CONVERTER 9a IN FIRST-STAGE CIRCUIT
SUB-A/D CONVERTER 9 IN SECOND-STAGE CIRCUIT
1001
1000
0111
0110
0101
0100
00
11
10
01
00
11
eR1
OR
eR2

(b)


SUB-A/D CONVERTER 9a IN FIRST-STAGE CIRCUIT
SUB-A/D CONVERTER 9 IN SECOND-STAGE CIRCUIT
1001
1000
0111
0110
0101
0100
00
11
10
01
00
11
eR1
OR
eR2

(c)


SUB-A/D CONVERTER 9a IN FIRST-STAGE CIRCUIT
SUB-A/D CONVERTER 9 IN SECOND-STAGE CIRCUIT
1001
1000
0111
0110
0101
0100
00
11
10
01
00
11
eR1
OR
eR2

(d)

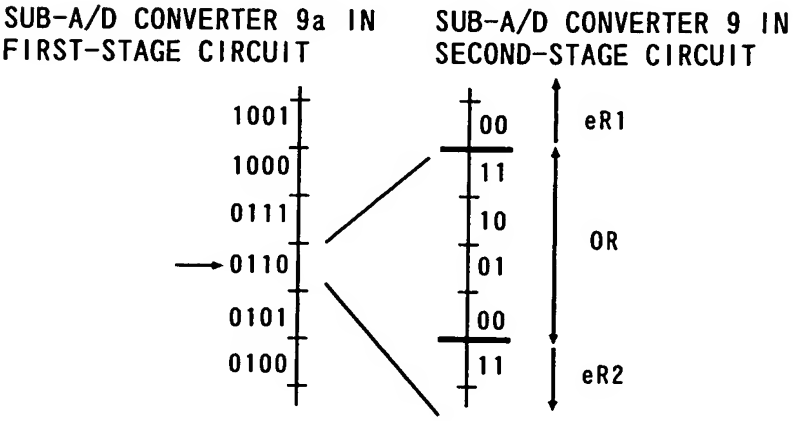

SUB-A/D CONVERTER 9a IN FIRST-STAGE CIRCUIT
SUB-A/D CONVERTER 9 IN SECOND-STAGE CIRCUIT
1001
1000
0111
0110
0101
0100
00
11
10
01
00
11
eR1
OR
eR2

FIG. 32

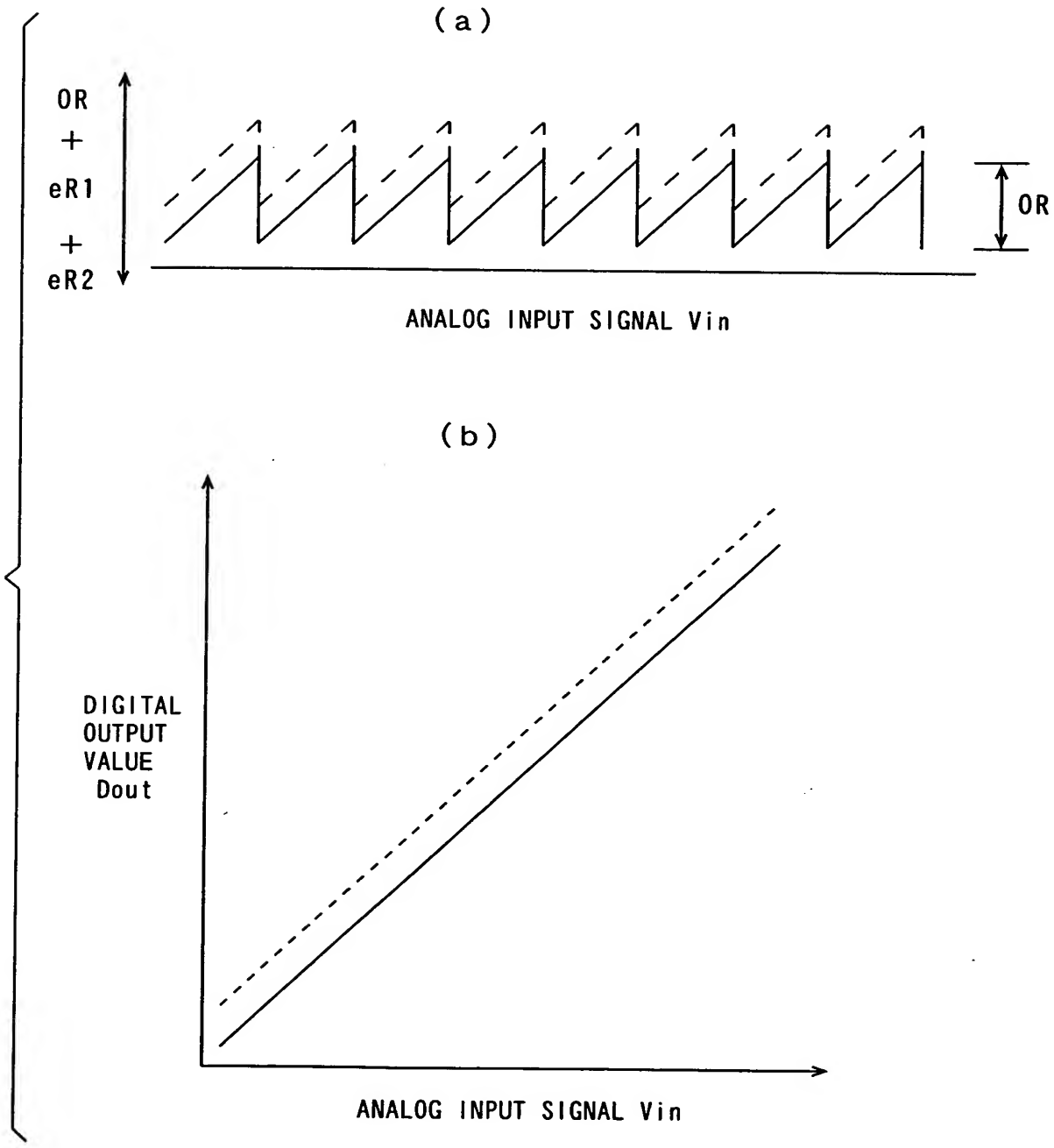

(a)
OR
+
eR1
+
eR2
OR
ANALOG INPUT SIGNAL Vin
(b)
DIGITAL
OUTPUT
VALUE
Dout
ANALOG INPUT SIGNAL Vin

FIG. 33

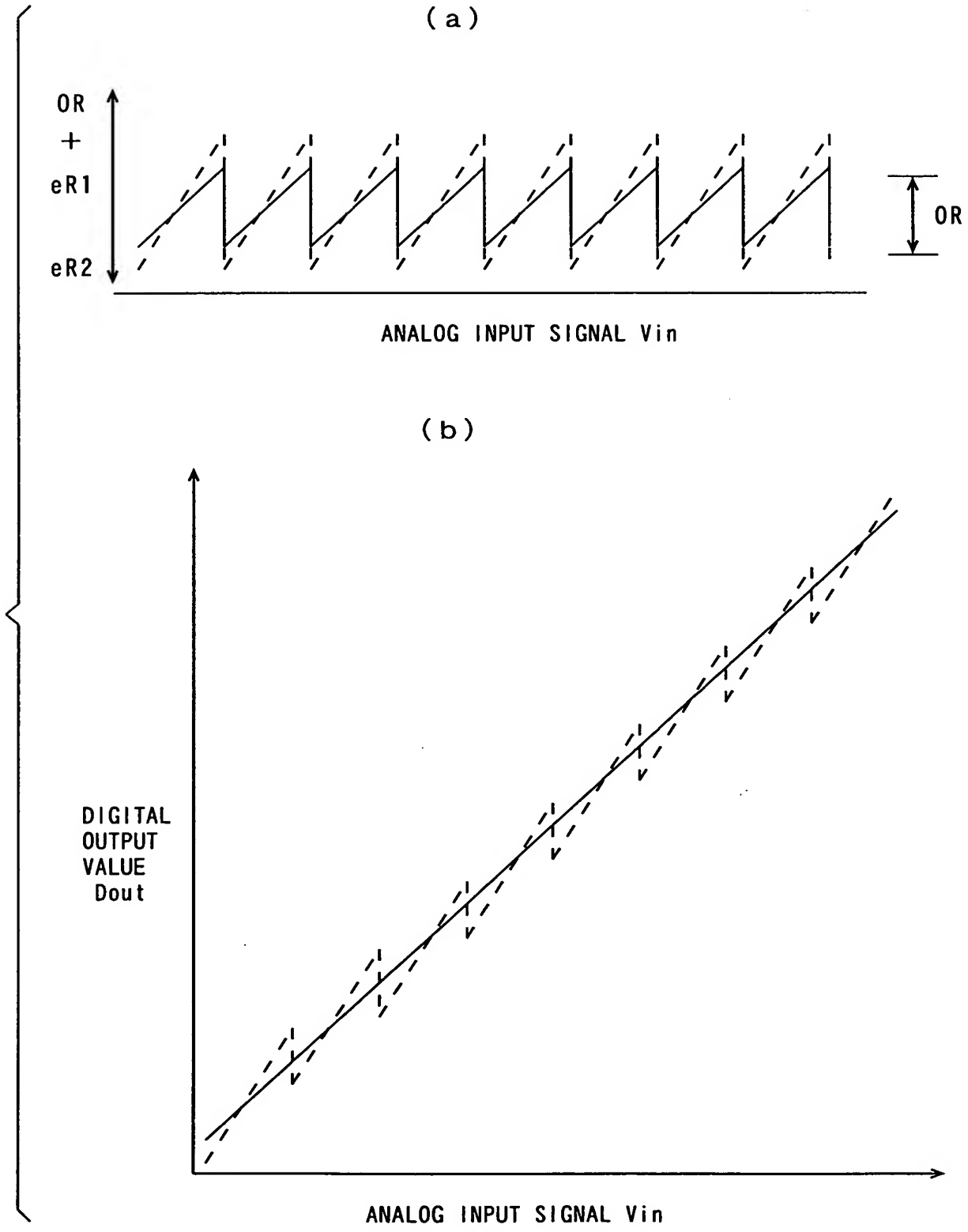

(a)
OR
+
eR1
eR2
OR
ANALOG INPUT SIGNAL Vin
(b)
DIGITAL
OUTPUT
VALUE
Dout
ANALOG INPUT SIGNAL Vin

FIG. 34

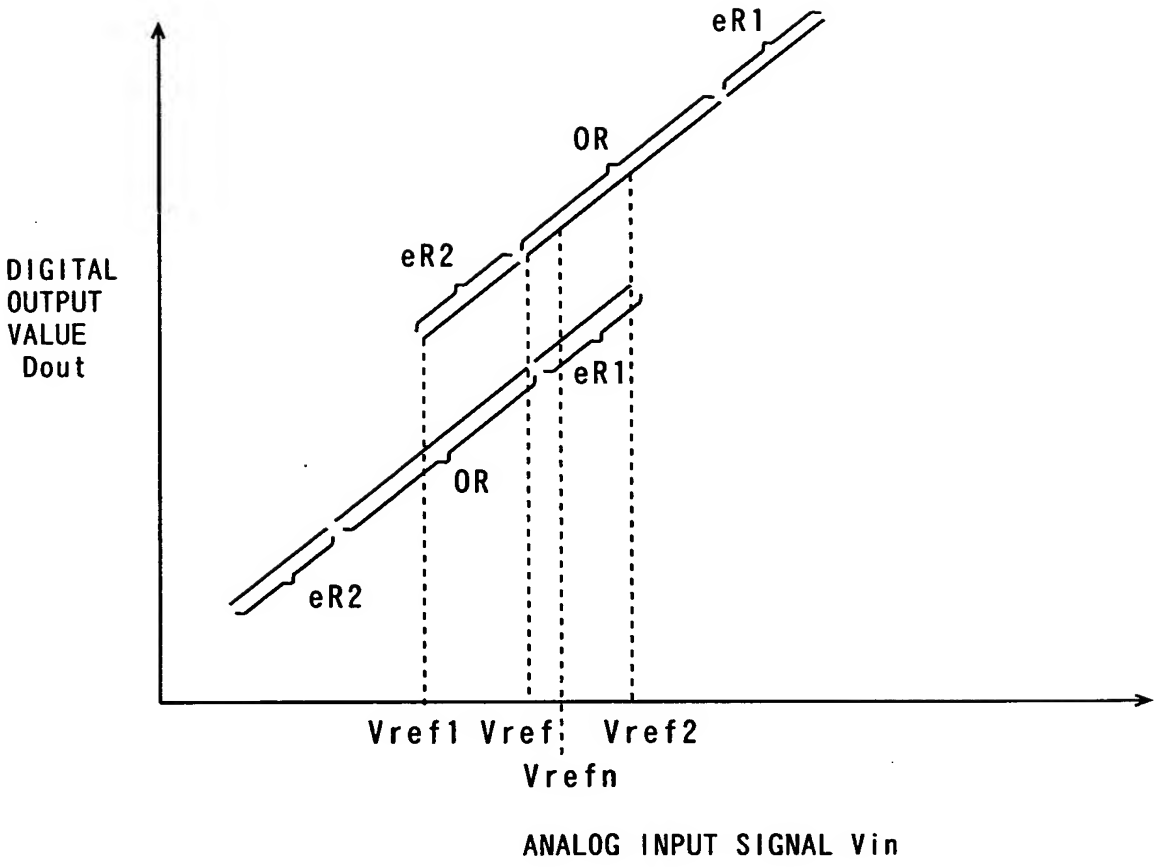

eR1
OR
eR2
DIGITAL
OUTPUT
VALUE
Dout
eR1
OR
eR2
Vref1 Vref Vref2
Vrefn
ANALOG INPUT SIGNAL Vin

FIG. 35 PRIOR ART

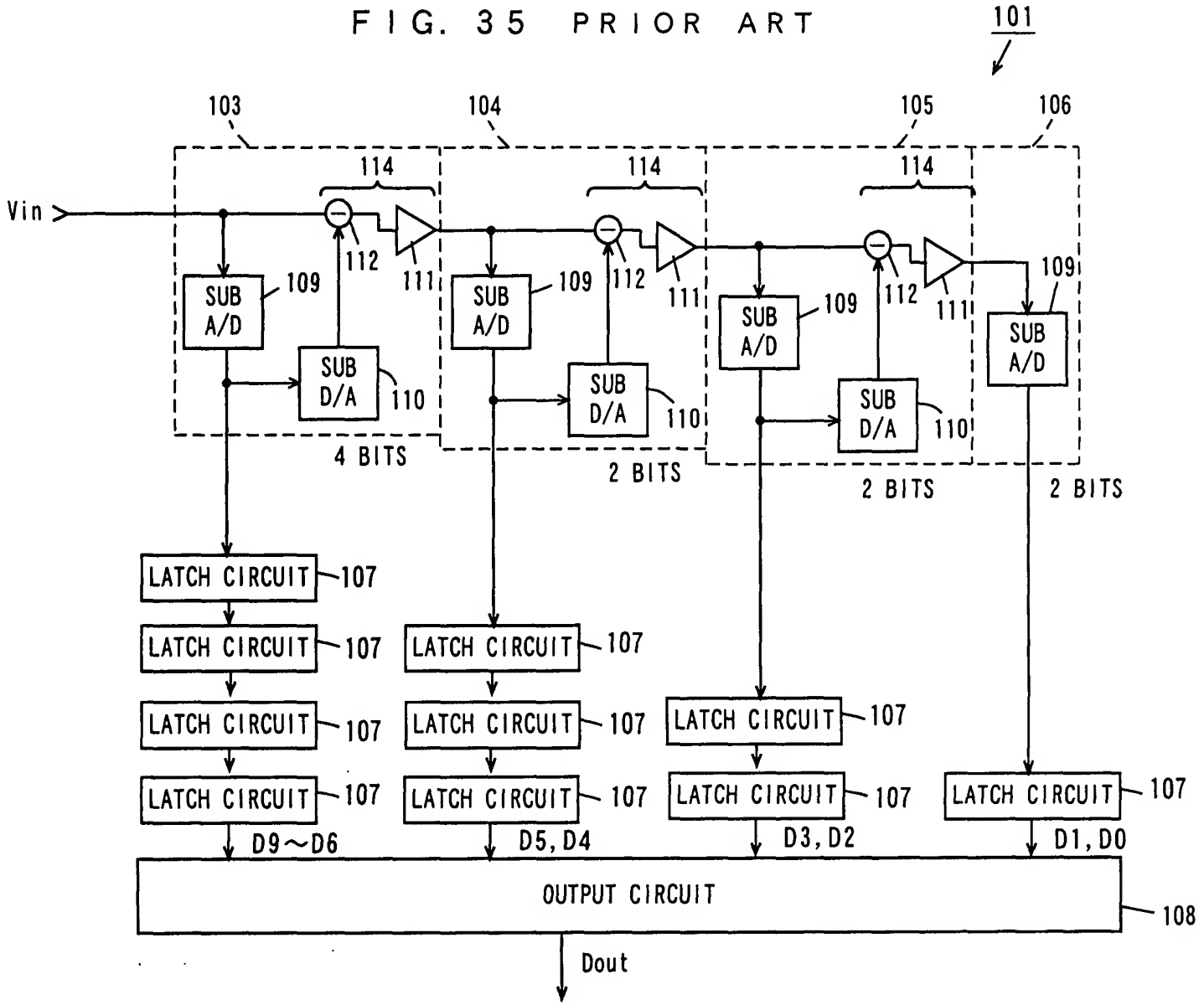


FIG. 36 PRIOR ART

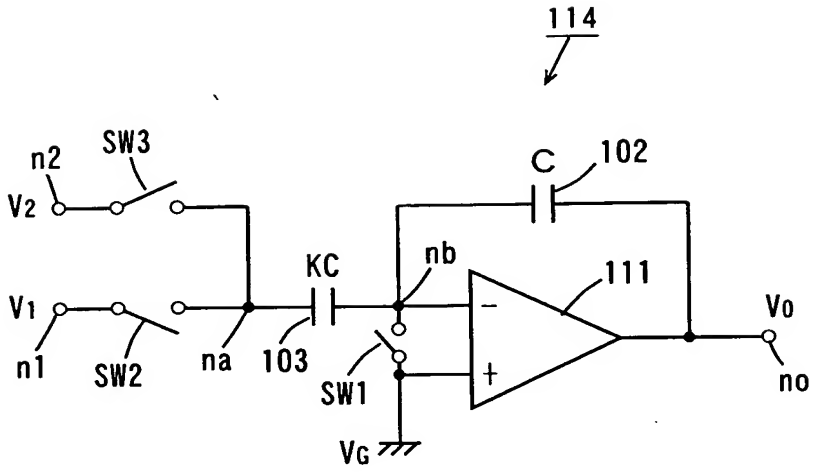


FIG. 37 PRIOR ART

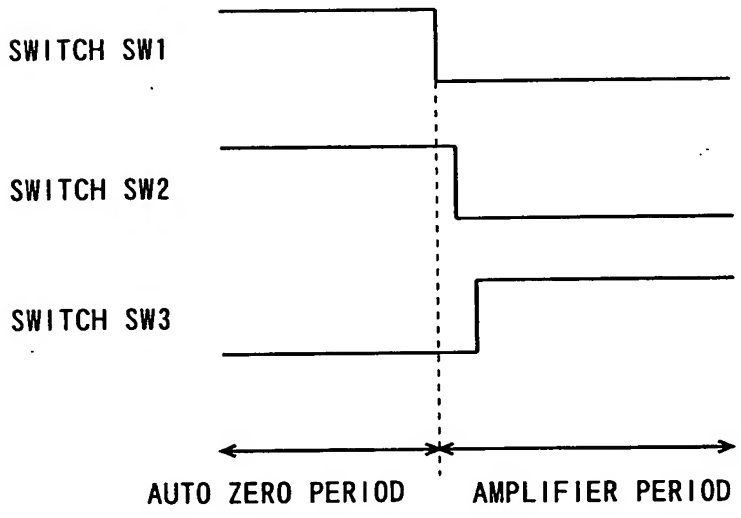


FIG. 38 PRIOR ART

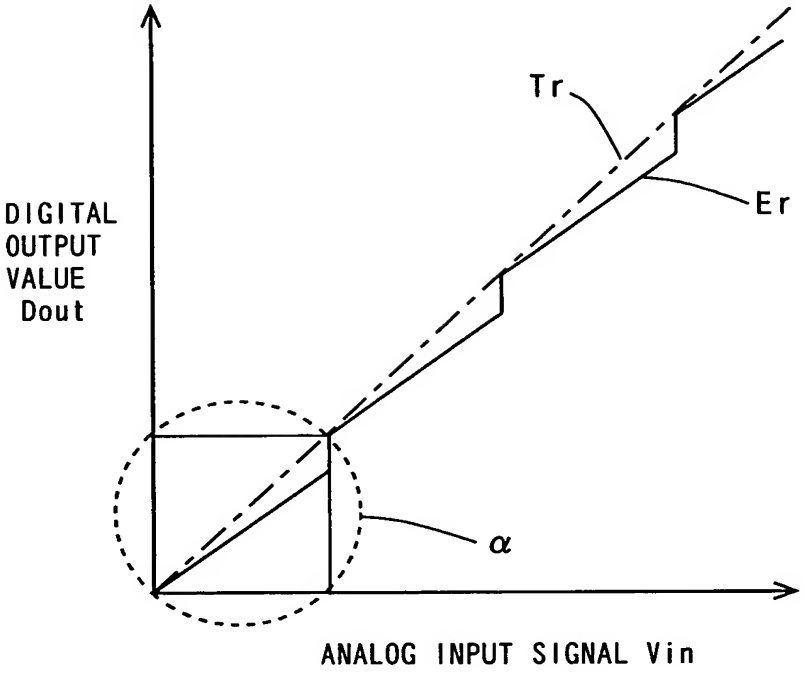


FIG. 39 PRIOR ART

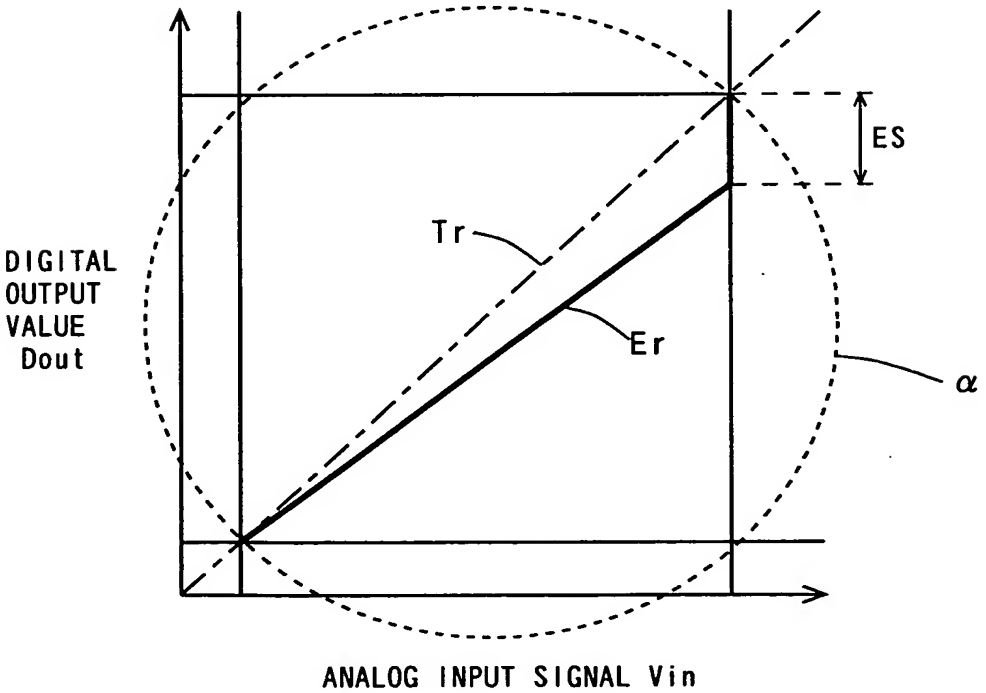


FIG. 40 PRIOR ART

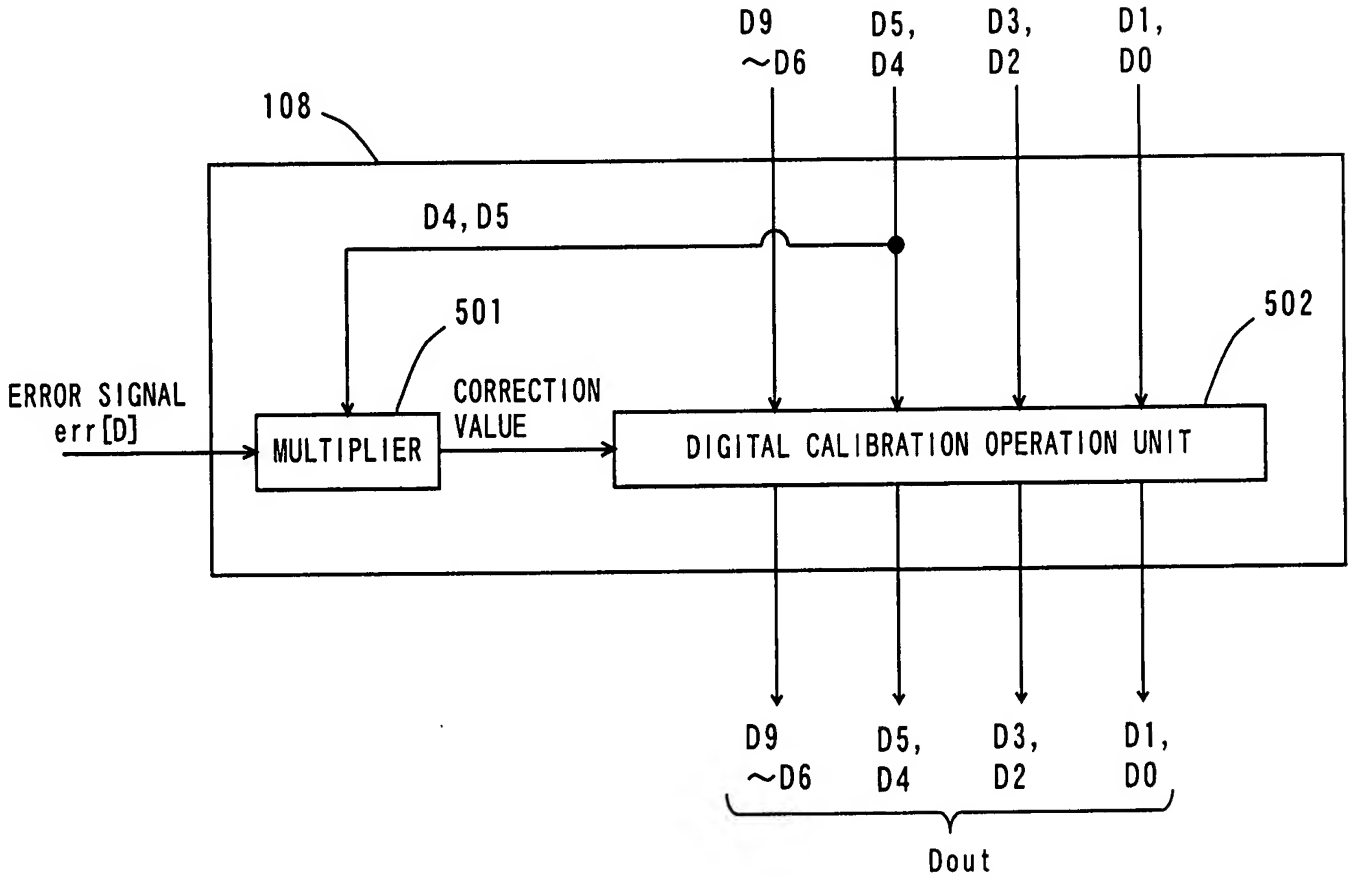


FIG. 41 PRIOR ART

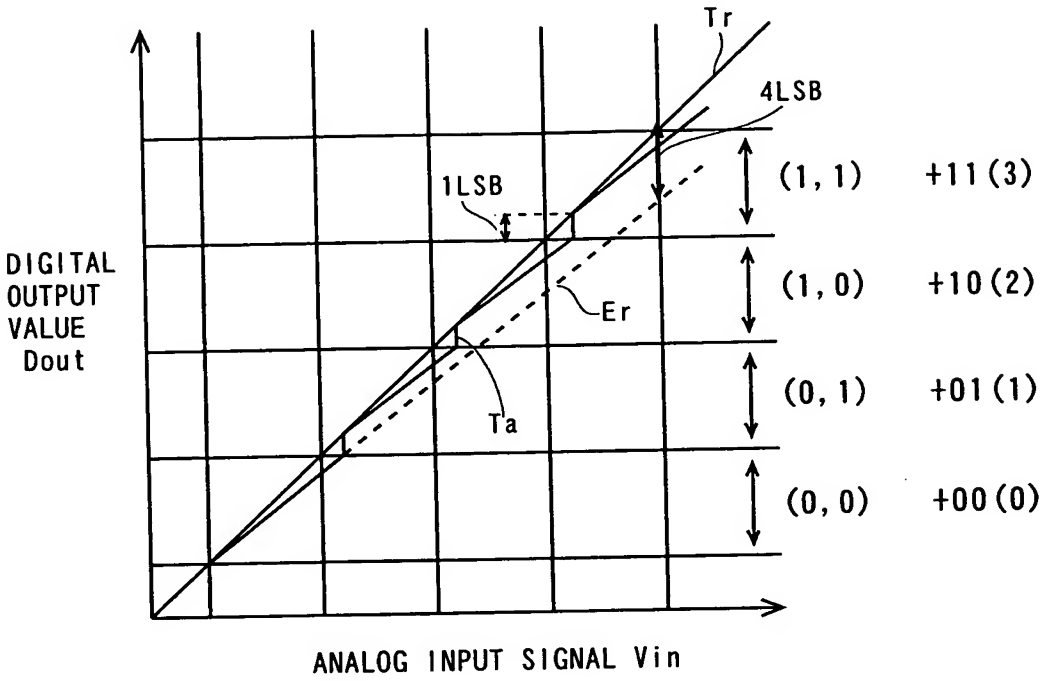


FIG. 42 PRIOR ART